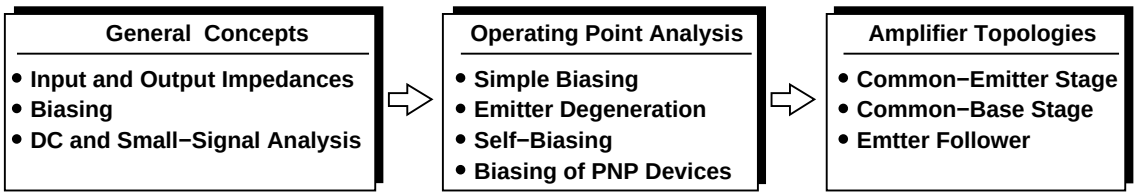
5

Bipolar Amplifiers

With the physics and operation of bipolar transistors described in Chapter 4, we now deal with amplifier circuits employing such devices. While the field of microelectronics involves much more than amplifiers, our study of cellphones and digital cameras in Chapter 1 indicates the extremely wide usage of amplification, motivating us to master the analysis and design of such building blocks. This chapter proceeds as follows.



Building the foundation for the remainder of this book, this chapter is quite long. Most of the concepts introduced here are invoked again in Chapter 7 (MOS amplifiers). The reader is therefore encouraged to take frequent breaks and absorb the material in small doses.

5.1 General Considerations

Recall from Chapter 4 that a voltage-controlled current source along with a load resistor can form an amplifier. In general, an amplifier produces an output (voltage or current) that is a magnified version of the input (voltage or current). Since most electronic circuits both sense and produce voltage quantities,[1] our discussion primarily centers around "voltage amplifiers" and the concept of "voltage gain," v_{out}/v_{in}.

What other aspects of an amplifier's performance are important? Three parameters that readily come to mind are (1) power dissipation (e.g., because it determines the battery lifetime in a cellphone or a digital camera); (2) speed (e.g., some amplifiers in a cellphone or analog-to-digital converters in a digital camera must operate at high frequencies); (3) noise (e.g., the front-end amplifier in a cellphone or a digital camera processes small signals and must introduce negligible noise of its own).

[1] Exceptions are described in Chapter 12.

5.1.1 Input and Output Impedances

In addition to the above parameters, the input and output (I/O) impedances of an amplifier play a critical role in its capability to interface with preceding and following stages. To understand this concept, let us first determine the I/O impedances of an *ideal* voltage amplifier. At the input, the circuit must operate as a voltmeter, i.e., sense a voltage without disturbing (loading) the preceding stage. The ideal input impedance is therefore infinite. At the output, the circuit must behave as a voltage source, i.e., deliver a constant signal level to any load impedance. Thus, the ideal output impedance is equal to zero.

In reality, the I/O impedances of a voltage amplifier may considerably depart from the ideal values, requiring attention to the interface with other stages. The following example illustrates the issue.

Example 5.1

An amplifier with a voltage gain of 10 senses a signal generated by a microphone and applies the amplified output to a speaker [Fig. 5.1(a)]. Assume the microphone can be modeled with a voltage source having a 10-mV peak-to-peak signal and a series resistance of 200 Ω. Also assume the speaker can be represented by an 8-Ω resistor.

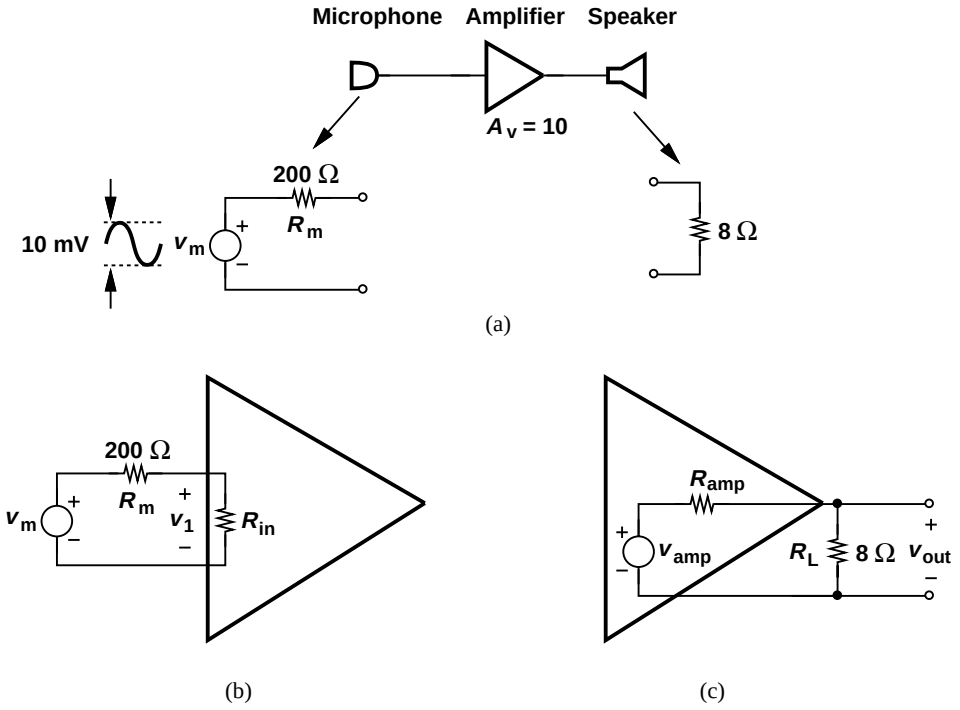


Figure 5.1 (a) Simple audio system, (b) signal loss due to amplifier input impedance, (c) signal loss due to amplifier output impedance.

(a) Determine the signal level sensed by the amplifier if the circuit has an input impedance of 2 kΩ or 500 Ω.

(b) Determine the signal level delivered to the speaker if the circuit has an output impedance of 10 Ω or 2 Ω.

Solution

(a) Figure 5.1(b) shows the interface between the microphone and the amplifier. The voltage

sensed by the amplifier is therefore given by

$$v_1 = \frac{R_{in}}{R_{in} + R_m} v_m. \tag{5.1}$$

For $R_{in} = 2$ kΩ,

$$v_1 = 0.91 v_m, \tag{5.2}$$

only 9% less than the microphone signal level. On the other hand, for $R_{in} = 500\,\Omega$,

$$v_1 = 0.71 v_m, \tag{5.3}$$

i.e., nearly 30% loss. It is therefore desirable to maximize the input impedance in this case.

(b) Drawing the interface between the amplifier and the speaker as in Fig. 5.1(c), we have

$$v_{out} = \frac{R_L}{R_L + R_{amp}} v_{amp}. \tag{5.4}$$

For $R_{amp} = 10\,\Omega$,

$$v_{out} = 0.44 v_{amp}, \tag{5.5}$$

a substantial attenuation. For $R_{amp} = 2\,\Omega$,

$$v_{out} = 0.8 v_{amp}. \tag{5.6}$$

Thus, the output impedance of the amplifier must be minimized.

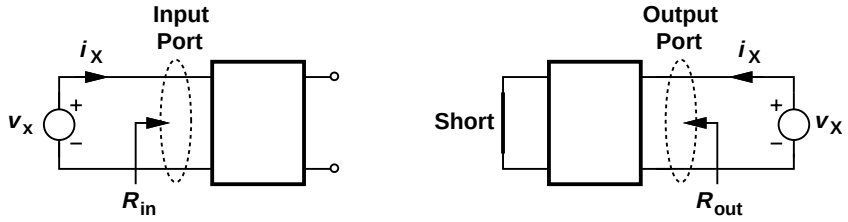
Exercise

If the signal delivered to the speaker is equal to $0.2v_m$, find the ratio of R_m and R_L.

The importance of I/O impedances encourages us to carefully prescribe the method of measuring them. As with the impedance of two-terminal devices such as resistors and capacitors, the input (output) impedance is measured between the input (output) nodes of the circuit while all independent sources in the circuit are set to zero.[2] Illustrated in Fig. 5.2, the method involves applying a voltage source to the two nodes (also called "port") of interest, measuring the resulting current, and defining v_X/i_X as the impedance. Also shown are arrows to denote "looking into" the input or output port and the corresponding impedance.

The reader may wonder why the output port in Fig. 5.2(a) is left open whereas the input port in Fig. 5.2(b) is shorted. Since a voltage amplifier is driven by a voltage source during normal operation, and since all independent sources must be set to zero, the input port in Fig. 5.2(b) must be shorted to represent a zero voltage source. That is, the procedure for calculating the output impedance is identical to that used for obtaining the Thevenin impedance of a circuit (Chapter 1). In Fig. 5.2(a), on the other hand, the output remains open because it is not connected to any external sources.

[2] Recall that a zero voltage source is replaced by a short and a zero current source by an open.



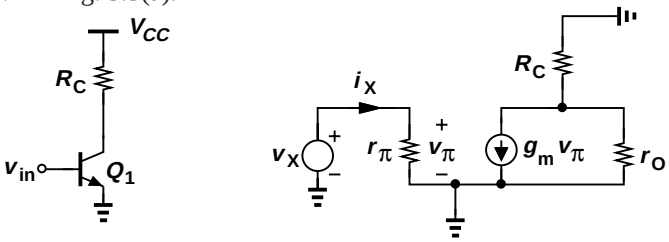
(a) (b)

Figure 5.2 Measurement of (a) input and (b) output impedances.

Determining the transfer of signals from one stage to the next, the I/O impedances are usually regarded as small-signal quantities—with the tacit assumption that the signal levels are indeed small. For example, the input impedance is obtained by applying a small change in the input voltage and measuring the resulting change in the input current. The small-signal models of semiconductor devices therefore prove crucial here.

Example 5.2

Assuming that the transistor operates in the forward active region, determine the input impedance of the circuit shown in Fig. 5.3(a).



(a) (b)

Figure 5.3 (a) Simple amplifier stage, (b) small-signal model.

Solution

Constructing the small-signal equivalent circuit depicted in Fig. 5.3(b), we note that the input impedance is simply given by

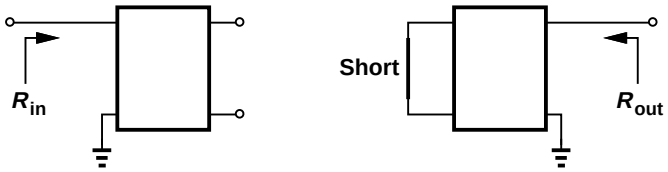
$$\frac{v_x}{i_x} = r_\pi. \tag{5.7}$$

Since $r_\pi = \beta/g_m = \beta V_T/I_C$, we conclude that a higher β or lower I_C yield a higher input impedance.

Exercise

What happens if R_C is doubled?

To simplify the notations and diagrams, we often refer to the impedance seen at a *node* rather than between two nodes (i.e., at a port). As illustrated in Fig. 5.4, such a convention simply assumes that the other node is the ground, i.e., the test voltage source is applied between the node of interest and ground.

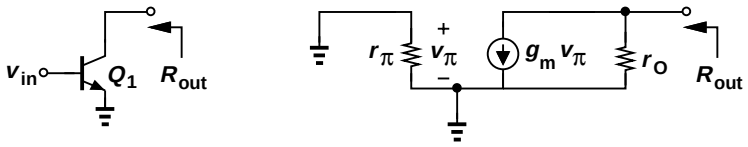


(a) (b)

Figure 5.4 Concept of impedance seen at a node.

Example 5.3

Calculate the impedance seen looking into the collector of Q_1 in Fig. 5.5(a).



(a) (b)

Figure 5.5 (a) Impedance seen at collector, (b) small-signal model.

Solution

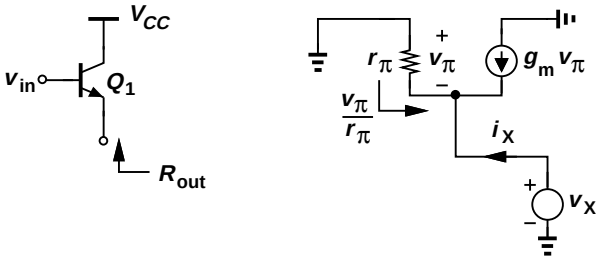
Setting the input voltage to zero and using the small-signal model in Fig. 5.5(b), we note that $v_\pi = 0$, $g_m v_\pi = 0$, and hence $R_{out} = r_O$.

Exercise

What happens if a resistance of value R_1 is placed in series with the base?

Example 5.4

Calculate the impedance seen at the emitter of Q_1 in Fig. 5.6(a). Neglect the Early effect for simplicity.



(a) (b)

Figure 5.6 (a) Impedance seen at emitter, (b) small-signal model.

Solution

Setting the input voltage to zero and replacing V_{CC} with ac ground, we arrive at the small-signal

circuit shown in Fig. 5.6(b). Interestingly, $v_\pi = -v_X$ and

$$g_m v_\pi + \frac{v_\pi}{r_\pi} = -i_X. \tag{5.8}$$

That is,

$$\frac{v_X}{i_X} = \frac{1}{g_m + \dfrac{1}{r_\pi}}. \tag{5.9}$$

Since $r_\pi = \beta/g_m \gg 1/g_m$, we have $R_{out} \approx 1/g_m$.

Exercise

What happens if a resistance of value R_1 is placed in series with the collector?

The above three examples provide three important rules that will be used throughout this book (Fig. 5.7): Looking into the base, we see r_π if the emitter is (ac) grounded. Looking into the collector, we see r_O if the emitter is (ac) grounded. Looking into the emitter, we see $1/g_m$ if the base is (ac) grounded and the Early effect is neglected. It is imperative that the reader master these rules and be able to apply them in more complex circuits.[3]

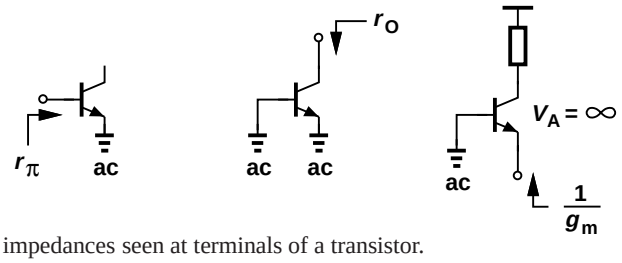


Figure 5.7 Summary of impedances seen at terminals of a transistor.

5.1.2 Biasing

Recall from Chapter 4 that a bipolar transistor operates as an amplifying device if it is biased in the active mode; that is, in the absence of signals, the environment surrounding the device must ensure that the base-emitter and base-collector junctions are forward- and reverse-biased, respectively. Moreover, as explained in Section 4.4, amplification properties of the transistor such as g_m, r_π, and r_O depend on the quiescent (bias) collector current. Thus, the surrounding circuitry must also set (define) the device bias currents properly.

5.1.3 DC and Small-Signal Analysis

The foregoing observations lead to a procedure for the analysis of amplifiers (and many other circuits). First, we compute the operating (quiescent) conditions (terminal voltages and currents) of each transistor in the absence of signals. Called the "dc analysis" or "bias analysis," this step determines both the region of operation (active or saturation) and the small-signal parameters of

[3] While beyond the scope of this book, it can be shown that the impedance seen at the emitter is approximately equal to $1/g_m$ only if the collector is tied to a relatively low impedance.

each device. Second, we perform "small-signal analysis," i.e., study the response of the circuit to small signals and compute quantities such as the voltage gain and I/O impedances. As an example, Fig. 5.8 illustrates the bias and signal components of a voltage and a current.

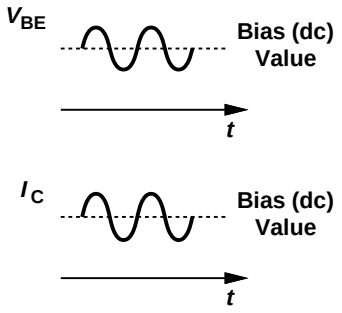


Figure 5.8 Bias and signal levels for a bipolar transistor.

It is important to bear in mind that small-signal analysis deals with only (small) *changes* in voltages and currents in a circuit around their quiescent values. Thus, as mentioned in Section 4.4.4, all *constant* sources, i.e., voltage and current sources that do not vary with time, must be set to zero for small-signal analysis. For example, the supply voltage is constant and, while establishing proper bias points, plays no role in the response to small signals. We therefore ground all constant voltage sources[4] and open all constant current sources while constructing the small-signal equivalent circuit. From another point of view, the two steps described above follow the superposition principle: first, we determine the effect of constant voltages and currents while signal sources are set to zero, and second, we analyze the response to signal sources while constant sources are set to zero. Figure 5.9 summarizes these concepts.

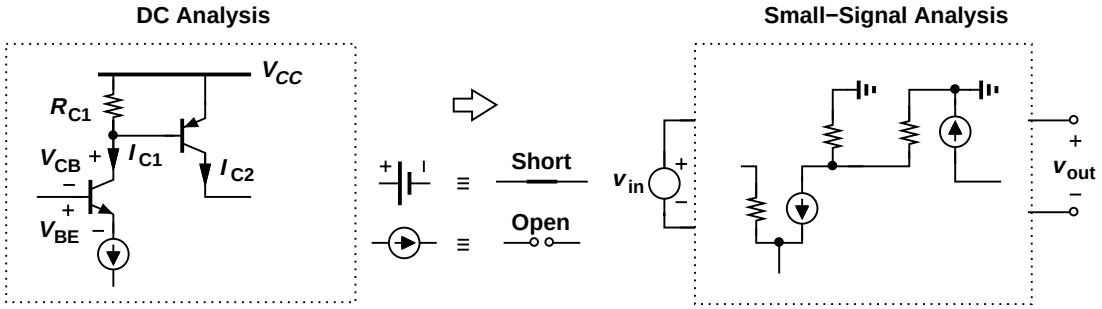


Figure 5.9 Steps in a general circuit analysis.

We should remark that the *design* of amplifiers follows a similar procedure . First, the circuitry around the transistor is designed to establish proper bias conditions and hence the necessary small-signal parameters. Second, the small- signal behavior of the circuit is studied to verify the required performance. Some iteration between the two steps may often be necessary so as to converge toward the desired behavior.

How do we differentiate between small-signal and large-signal operations? In other words, under what conditions can we represent the devices with their small-signal models? If the signal perturbs the bias point of the device only negligibly, we say the circuit operates in the small-signal regime. In Fig. 5.8, for example, the change in I_C due to the signal must remain small. This criterion is justified because the amplifying properties of the transistor such as g_m and r_π are

[4] We say all constant voltage sources are replaced by an "ac ground."

considered *constant* in small-signal analysis even though they in fact vary as the signal perturbs I_C. That is, a *linear* representation of the transistor holds only if the small-signal parameters themselves vary negligibly. The definition of "negligibly" somewhat depends on the circuit and the application, but as a rule of thumb, we consider 10% variation in the collector current as the upper bound for small-signal operation.

In drawing circuit diagrams hereafter, we will employ some simplified notations and symbols. Illustrated in Fig. 5.10 is an example where the battery serving as the supply voltage is replaced with a horizontal bar labeled V_{CC}.[5] Also, the input voltage source is simplified to one node called V_{in}, with the understanding that the other node is ground.

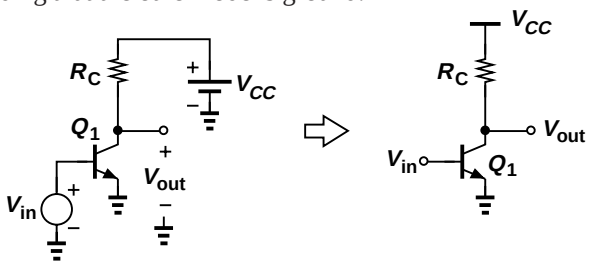


Figure 5.10 Notation for supply voltage.

In this chapter, we begin with the DC analysis and design of bipolar stages, developing skills to determine or create bias conditions. This phase of our study requires no knowledge of signals and hence the input and output ports of the circuit. Next, we introduce various amplifier topologies and examine their small-signal behavior.

5.2 Operating Point Analysis and Design

It is instructive to begin our treatment of operating points with an example.

Example 5.5

A student familiar with bipolar devices constructs the circuit shown in Fig. 5.11 and attempts to amplify the signal produced by a microphone. If $I_S = 6 \times 10^{-16}$ A and the peak value of the microphone signal is 20 mV, determine the peak value of the output signal.

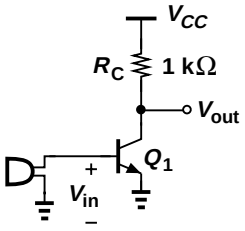


Figure 5.11 Amplifier driven directly by a microphone.

Solution

Unfortunately, the student has forgotten to bias the transistor. (The microphone does not produce a dc output). If V_{in} $(= V_{BE})$ reaches 20 mV, then

$$\Delta I_C = I_S \exp \frac{\Delta V_{BE}}{V_T} \tag{5.10}$$

[5] The subscript CC indicates supply voltage feeding the collector.

$$= 1.29 \times 10^{-15}\ \text{A}. \tag{5.11}$$

This change in the collector current yields a change in the output voltage equal to

$$R_C \Delta I_C = 1.29 \times 10^{-12}\ \text{V}. \tag{5.12}$$

The circuit generates virtually no output because the bias current (in the absence of the microphone signal) is zero and so is the transconductance.

Exercise

Repeat the above example if a constant voltage of 0.65 V is placed in series with the microphone.

As mentioned in Section 5.1.2, biasing seeks to fulfill two objectives: ensure operation in the forward active region, and set the collector current to the value required in the application. Let us return to the above example for a moment.

Example 5.6

Having realized the bias problem, the student in Example 5.5 modifies the circuit as shown in Fig. 5.12, connecting the base to V_{CC} to allow dc biasing for the base-emitter junction. Explain why the student needs to learn more about biasing.

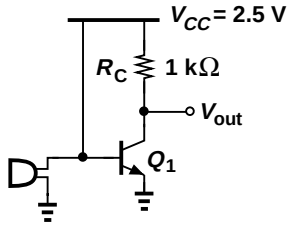


Figure 5.12 Amplifier with base tied to V_{CC}.

Solution

The fundamental issue here is that the signal generated by the microphone is *shorted* to V_{CC}. Acting as an ideal voltage source, V_{CC} maintains the base voltage at a *constant* value, prohibiting any change introduced by the microphone. Since V_{BE} remains constant, so does V_{out}, leading to no amplification.

Another important issue relates to the value of V_{BE}: with $V_{BE} = V_{CC} = 2.5$ V, enormous currents flow into the transistor.

Exercise

Does the circuit operate better if a resistor is placed in series with the emitter of Q_1?

5.2.1 Simple Biasing

Now consider the topology shown in Fig. 5.13, where the base is tied to V_{CC} through a relatively large resistor, R_B, so as to forward-bias the base-emitter junction. Our objective is to determine the terminal voltages and currents of Q_1 and obtain the conditions that ensure biasing in the active mode. How do we analyze this circuit? One can replace Q_1 with its large-signal model and apply KVL and KCL, but the resulting nonlinear equation(s) yield little intuition. Instead, we recall that the base-emitter voltage in most cases falls in the range of 700 to 800 mV and can be considered relatively constant. Since the voltage drop across R_B is equal to $R_B I_B$, we have

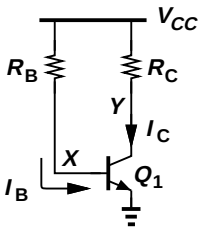


Figure 5.13 Use of base resistance for base current path.

$$R_B I_B + V_{BE} = V_{CC} \tag{5.13}$$

and hence

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}. \tag{5.14}$$

With the base current known, we write

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B}, \tag{5.15}$$

note that the voltage drop across R_C is equal to $R_C I_C$, and hence obtain V_{CE} as

$$V_{CE} = V_{CC} - R_C I_C \tag{5.16}$$

$$= V_{CC} - \beta \frac{V_{CC} - V_{BE}}{R_B} R_C. \tag{5.17}$$

Calculation of V_{CE} is necessary as it reveals whether the device operates in the active mode or not. For example, to avoid saturation completely, we require the collector voltage to remain above the base voltage:

$$V_{CC} - \beta \frac{V_{CC} - V_{BE}}{R_B} R_C > V_{BE}. \tag{5.18}$$

The circuit parameters can therefore be chosen so as to guarantee this condition.

In summary, using the sequence $I_B \rightarrow I_C \rightarrow V_{CE}$, we have computed the important terminal currents and voltages of Q_1. While not particularly interesting here, the emitter current is simply equal to $I_C + I_B$.

The reader may wonder about the error in the above calculations due to the assumption of a constant V_{BE} in the range of 700 to 800 mV. An example clarifies this issue.

Example 5.7

For the circuit shown in Fig. 5.14, determine the collector bias current. Assume $\beta = 100$ and $I_S = 10^{-17}$ A. Verify that Q_1 operates in the forward active region.

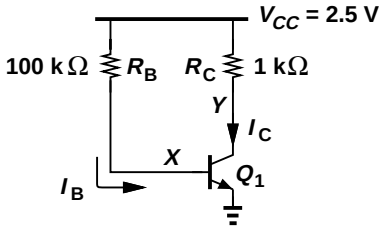


Figure 5.14 Simple biased stage.

Solution

Since I_S is relatively small, we surmise that the base-emitter voltage required to carry typical current level is relatively large. Thus, we use $V_{BE} = 800$ mV as an initial guess and write Eq. (5.14) as

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{5.19}$$

$$\approx 17\ \mu\text{A}. \tag{5.20}$$

It follows that

$$I_C = 1.7\ \text{mA}. \tag{5.21}$$

With this result for I_C, we calculate a new value for V_{BE}:

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \tag{5.22}$$

$$= 852\ \text{mV}, \tag{5.23}$$

and iterate to obtain more accurate results. That is,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{5.24}$$

$$= 16.5\ \mu\text{A} \tag{5.25}$$

and hence

$$I_C = 1.65\ \text{mA}. \tag{5.26}$$

Since the values given by (5.21) and (5.26) are quite close, we consider $I_C = 1.65$ mA accurate enough and iterate no more.

Writing (5.16), we have

$$V_{CE} = V_{CC} - R_C I_C \tag{5.27}$$

$$= 0.85\ \text{V}, \tag{5.28}$$

a value nearly equal to V_{BE}. The transistor therefore operates near the edge of active and saturation modes.

Exercise

What value of R_B provides a reverse bias of 200 mV across the base-collector junction?

The biasing scheme of Fig. 5.13 merits a few remarks. First, the effect of V_{BE} "uncertainty" becomes more pronounced at low values of V_{CC} because $V_{CC}-V_{BE}$ determines the base current. Thus, in low-voltage design—an increasingly common paradigm in modern electronic systems—the bias is more sensitive to V_{BE} variations among transistors or with temperature . Second, we recognize from Eq. (5.15) that I_C heavily depends on β, a parameter that may change considerably. In the above example, if β increases from 100 to 120, then I_C rises to 1.98 mA and V_{CE} falls to 0.52, driving the transistor toward heavy saturation. For these reasons, the topology of Fig. 5.13 is rarely used in practice.

5.2.2 Resistive Divider Biasing

In order to suppress the dependence of I_C upon β, we return to the fundamental relationship $I_C = I_S \exp(V_{BE}/V_T)$ and postulate that I_C must be set by applying a well-defined V_{BE}. Figure 5.15 depicts an example, where R_1 and R_2 act as a voltage divider, providing a base-emitter voltage equal to

$$V_X = \frac{R_2}{R_1 + R_2} V_{CC}, \tag{5.29}$$

if the base current is negligible. Thus,

$$I_C = I_S \exp\left(\frac{R_2}{R_1 + R_2} \cdot \frac{V_{CC}}{V_T}\right), \tag{5.30}$$

a quantity independent of β. Nonetheless, the design must ensure that the base current remains negligible.

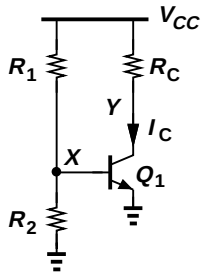


Figure 5.15 Use of resistive divider to define V_{BE}.

Example 5.8

Determine the collector current of Q_1 in Fig. 5.16 if $I_S = 10^{-17}$ A and $\beta = 100$. Verify that the base current is negligible and the transistor operates in the active mode.

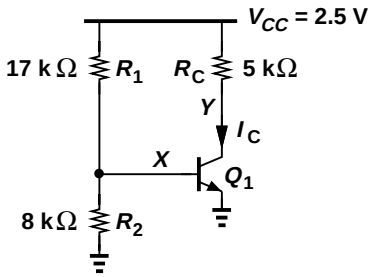


Figure 5.16 Example of biased stage.

Solution

Neglecting the base current of Q_1, we have

$$V_X = \frac{R_2}{R_1 + R_2} V_{CC} \tag{5.31}$$

$$= 800\ \text{mV}. \tag{5.32}$$

It follows that

$$I_C = I_S \exp \frac{V_{BE}}{V_T} \tag{5.33}$$

$$= 231\ \mu\text{A} \tag{5.34}$$

and

$$I_B = 2.31\ \mu\text{A}. \tag{5.35}$$

Is the base current negligible? With which quantity should this value be compared? Provided by the resistive divider, I_B must be negligible with respect to the current flowing through R_1 and R_2:

$$I_B \overset{?}{\ll} \frac{V_{CC}}{R_1 + R_2}. \tag{5.36}$$

This condition indeed holds in this example because $V_{CC}/(R_1 + R_2) = 100\ \mu\text{A} \approx 43 I_B$.

We also note that

$$V_{CE} = 1.345\ \text{V}, \tag{5.37}$$

and hence Q_1 operates in the active region.

Exercise

What is the maximum value of R_C if Q_1 must remain in soft saturation?

The analysis approach taken in the above example assumes a negligible base current, requiring verification at the end. But what if the end result indicates that I_B is *not* negligible? We now analyze the circuit without this assumption. Let us replace the voltage divider with a Thevenin

equivalent (Fig. 5.17); noting that V_{Thev} is equal to the open-circuit output voltage (V_X when the amplifier is disconnected):

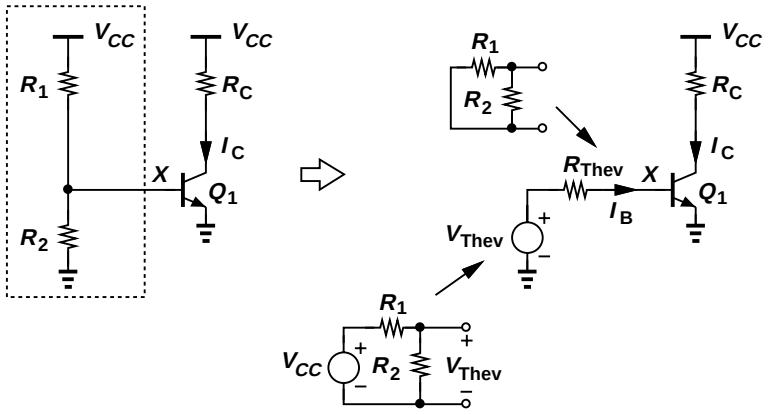


Figure 5.17 Use of Thevenin equivalent to calculate bias.

$$V_{Thev} = \frac{R_2}{R_1 + R_2} V_{CC}. \tag{5.38}$$

Moreover, R_{Thev} is given by the output resistance of the network if V_{CC} is set to zero:

$$R_{Thev} = R_1 || R_2. \tag{5.39}$$

The simplified circuit yields:

$$V_X = V_{Thev} - I_B R_{Thev} \tag{5.40}$$

and

$$I_C = I_S \exp \frac{V_{Thev} - I_B R_{Thev}}{V_T}. \tag{5.41}$$

This result along with $I_C = \beta I_B$ forms the system of equations leading to the values of I_C and I_B. As in the previous examples, iterations prove useful here, but the exponential dependence in Eq. (5.41) gives rise to wide fluctuations in the intermediate solutions. For this reason, we rewrite (5.41) as

$$I_B = \left(V_{Thev} - V_T \ln \frac{I_C}{I_S} \right) \cdot \frac{1}{R_{Thev}}, \tag{5.42}$$

and begin with a guess for $V_{BE} = V_T \ln(I_C/I_S)$. The iteration then follows the sequence $V_{BE} \rightarrow I_B \rightarrow I_C \rightarrow V_{BE} \rightarrow \cdots$.

Example 5.9

Calculate the collector current of Q_1 in Fig. 5.18(a). Assume $\beta = 100$ and $I_S = 10^{-17}$ A.

Solution

Constructing the equivalent circuit shown in Fig. 5.18(b), we note that

$$V_{Thev} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{5.43}$$

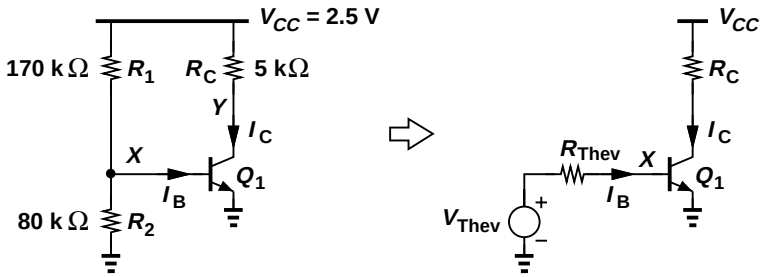


Figure 5.18 (a) Stage with resistive divider bias, (b) stage with Thevenin equivalent for the resistive divider and V_{CC}.

$$= 800\,\text{mV} \tag{5.44}$$

and

$$R_{Thev} = R_1||R_2 \tag{5.45}$$

$$= 54.4\,\text{k}\Omega. \tag{5.46}$$

We begin the iteration with an initial guess $V_{BE} = 750$ mV (because we know that the voltage drop across R_{Thev} makes V_{BE} *less* than V_{Thev}), thereby arriving at the base current:

$$I_B = \frac{V_{Thev} - V_{BE}}{R_{Thev}} \tag{5.47}$$

$$= 0.919\,\mu\text{A}. \tag{5.48}$$

Thus, $I_C = \beta I_B = 91.9\,\mu$A and

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \tag{5.49}$$

$$= 776\,\text{mV}. \tag{5.50}$$

It follows that $I_B = 0.441\,\mu$A and hence $I_C = 44.1\,\mu$A, still a large fluctuation with respect to the first value from above. Continuing the iteration, we obtain $V_{BE} = 757$ mV, $I_B = 0.79\,\mu$A and $I_C = 79.0\,\mu$A. After many iterations, $V_{BE} \approx 766$ mV and $I_C = 63\,\mu$A.

Exercise

How much can R_2 be increased if Q_1 must remain in soft saturation?

While proper choice of R_1 and R_2 in the topology of Fig. 5.15 makes the bias relatively insensitive to β, the exponential dependence of I_C upon the voltage generated by the resistive divider still leads to substantial bias variations. For example, if R_2 is 1% higher than its nominal value, so is V_X, thus multiplying the collector current by $\exp(0.01 V_{BE}/V_T) \approx 1.36$ (for $V_{BE} = 800$ mV). In other words, a 1% error in one resistor value introduces a 36% error in the collector current. The circuit is therefore still of little practical value.

5.2.3 Biasing with Emitter Degeneration

A biasing configuration that alleviates the problem of sensitivity to β and V_{BE} is shown in Fig. 5.19. Here, resistor R_E appears in series with the emitter, thereby lowering the sensitivity to V_{BE}. From an intuitive viewpoint, this occurs because R_E exhibits a *linear* (rather than exponential) I-V relationship. Thus, an error in V_X due to inaccuracies in R_1, R_2, or V_{CC} is partly "absorbed" by R_E, introducing a smaller error in V_{BE} and hence I_C. Called "emitter degeneration," the

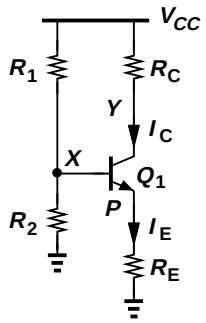


Figure 5.19 Addition of degeneration resistor to stabilize bias point.

addition of R_E in series with the emitter alters many attributes of the circuit, as described later in this chapter.

To understand the above property, let us determine the bias currents of the transistor. Neglecting the base current, we have $V_X = V_{CC}R_2/(R_1 + R_2)$. Also, $V_P = V_X - V_{BE}$, yielding

$$I_E = \frac{V_P}{R_E} \tag{5.51}$$

$$= \frac{1}{R_E}\left(V_{CC}\frac{R_2}{R_1 + R_2} - V_{BE}\right) \tag{5.52}$$

$$\approx I_C, \tag{5.53}$$

if $\beta \gg 1$. How can this result be made less sensitive to V_X or V_{BE} variations? If the voltage drop across R_E, i.e., the difference between $V_{CC}R_2/(R_1 + R_2)$ and V_{BE} is large enough to absorb and swamp such variations, then I_E and I_C remain relatively constant. An example illustrates this point.

Example 5.10

Calculate the bias currents in the circuit of Fig. 5.20 and verify that Q_1 operates in the forward active region. Assume $\beta = 100$ and $I_S = 5 \times 10^{-17}$ A. How much does the collector current change if R_2 is 1% higher than its nominal value?

Solution

We neglect the base current and write

$$V_X = V_{CC}\frac{R_2}{R_1 + R_2} \tag{5.54}$$

$$= 900\ \text{mV}. \tag{5.55}$$

Using $V_{BE} = 800$ mV as an initial guess, we have

$$V_P = V_X - V_{BE} \tag{5.56}$$

$$= 100\ \text{mV}, \tag{5.57}$$

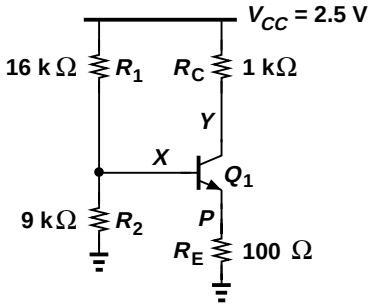


Figure 5.20 Example of biased stage.

and hence

$$I_E \approx I_C \approx 1 \text{ mA}. \tag{5.58}$$

With this result, we must reexamine the assumption of $V_{BE} = 800$ mV. Since

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \tag{5.59}$$

$$= 796 \text{ mV}, \tag{5.60}$$

we conclude that the initial guess is reasonable. Furthermore, Eq. (5.57) suggests that a 4-mV error in V_{BE} leads to a 4% error in V_P and hence I_E, indicating a good approximation.

Let us now determine if Q_1 operates in the active mode. The collector voltage is given by

$$V_Y = V_{CC} - I_C R_C \tag{5.61}$$

$$= 1.5 \text{ V}. \tag{5.62}$$

With the base voltage at 0.9 V, the device is indeed in the active region.

Is the assumption of negligible base current valid? With $I_C \approx 1$ mA, $I_B \approx 10\,\mu$A whereas the current flowing through R_1 and R_2 is equal to 100 μA. The assumption is therefore reasonable. For greater accuracy, an iterative procedure similar to that in Example 5.9 can be followed.

If R_2 is 1% higher than its nominal value, then (5.54) indicates that V_X rises to approximately 909 mV. We may assume that the 9-mV change directly appears across R_E, raising the emitter current by $9 \text{ mV}/100\,\Omega = 90\,\mu$A. From Eq. (5.56), we note that this assumption is equivalent to considering V_{BE} constant, which is reasonable because the emitter and collector currents have changed by only 9%.

Exercise

What value of R_2 places Q_1 at the edge of saturation?

The bias topology of Fig. 5.19 is used extensively in discrete circuits and occasionally in integrated circuits. Illustrated in Fig. 5.21, two rules are typically followed: (1) $I_1 \gg I_B$ to lower sensitivity to β, and (2) V_{RE} must be large enough (100 mV to several hundred millivolts) to suppress the effect of uncertainties in V_X and V_{BE}.

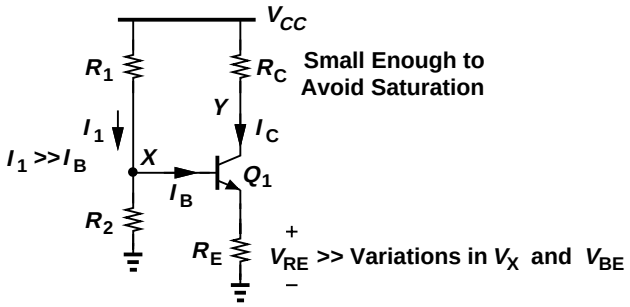


Figure 5.21 Summary of robust bias conditions.

Design Procedure It is possible to prescribe a design procedure for the bias topology of Fig. 5.21 that serves most applications: (1) decide on a collector bias current that yields proper small-signal parameters such as g_m and r_π; (2) based on the expected variations of R_1, R_2, and V_{BE}, choose a value for $V_{RE} \approx I_C R_E$, e.g., 200 mV; (3) calculate $V_X = V_{BE} + I_C R_E$ with $V_{BE} = V_T \ln(I_C/I_S)$; (4) choose R_1 and R_2 so as to provide the necessary value of V_X *and* establish $I_1 \gg I_B$. Determined by small-signal gain requirements, the value of R_C is bounded by a maximum that places Q_1 at the edge of saturation. The following example illustrates these concepts.

Example 5.11

Design the circuit of Fig. 5.21 so as to provide a transconductance of $1/(52\ \Omega)$ for Q_1. Assume $V_{CC} = 2.5$ V, $\beta = 100$, and $I_S = 5 \times 10^{-17}$ A. What is the maximum tolerable value of R_C?

Solution

A g_m of $(52\ \Omega)^{-1}$ translates to a collector current of 0.5 mA and a V_{BE} of 778 mV. Assuming $R_E I_C = 200$ mV, we obtain $R_E = 400\ \Omega$. To establish $V_X = V_{BE} + R_E I_C = 978$ mV, we must have

$$\frac{R_2}{R_1 + R_2} V_{CC} = V_{BE} + R_E I_C, \tag{5.63}$$

where the base current is neglected. For the base current $I_B = 5\ \mu$A to be negligible,

$$\frac{V_{CC}}{R_1 + R_2} \gg I_B, \tag{5.64}$$

e.g., by a factor of 10. Thus, $R_1 + R_2 = 50$ kΩ, which in conjunction with (5.63) yields

$$R_1 = 30.45\ \text{k}\Omega \tag{5.65}$$

$$R_2 = 19.55\ \text{k}\Omega. \tag{5.66}$$

How large can R_C be? Since the collector voltage is equal to $V_{CC} - R_C I_C$, we pose the following constraint to ensure active mode operation:

$$V_{CC} - R_C I_C > V_X; \tag{5.67}$$

that is,

$$R_C I_C < 1.522\ \text{V}. \tag{5.68}$$

Consequently,

$$R_C < 3.044\,\text{k}\Omega. \tag{5.69}$$

If R_C exceeds this value, the collector voltage falls below the base voltage. As mentioned in Chapter 4, the transistor can tolerate soft saturation, i.e., up to about 400 mV of base-collector forward bias. Thus, in low-voltage applications, we may allow $V_Y \approx V_X - 400\,\text{mV}$ and hence a greater value for R_C.

Exercise

Repeat the above example if the power budget is only 1 mW and the transconductance of Q_1 is not given.

The two rules depicted in Fig. 5.21 to lower sensitivities do impose some trade-offs. Specifically, an overly conservative design faces the following issues: (1) if we wish I_1 to be much much greater than I_B, then $R_1 + R_2$ and hence R_1 and R_2 are quite small, leading to a low *input impedance*; (2) if we choose a very large V_{RE}, then V_X ($= V_{BE} + V_{RE}$) must be high, thereby limiting the minimum value of the collector voltage to avoid saturation. Let us return to the above example and study these issues.

Example 5.12

Repeat Example 5.11 but assuming $V_{RE} = 500$ mV and $I_1 \geq 100 I_B$.

Solution

The collector current and base-emitter voltage remain unchanged. The value of R_E is now given by $500\,\text{mV}/0.5\,\text{mA} = 1\,\text{k}\Omega$. Also, $V_X = V_{BE} + R_E I_C = 1.278$ V and (5.63) still holds. We rewrite (5.64) as

$$\frac{V_{CC}}{R_1 + R_2} \geq 100 I_B, \tag{5.70}$$

obtaining $R_1 + R_2 = 5\,\text{k}\Omega$. It follows that

$$R_1 = 1.45\,\text{k}\Omega \tag{5.71}$$

$$R_2 = 3.55\,\text{k}\Omega. \tag{5.72}$$

Since the base voltage has risen to 1.278 V, the collector voltage must exceed this value to avoid saturation, leading to

$$R_C < \frac{V_{CC} - V_X}{I_C} \tag{5.73}$$

$$< 1.044\,\text{k}\Omega. \tag{5.74}$$

As seen in Section 5.3.1, the reduction in R_C translates to a lower voltage gain. Also, the much smaller values of R_1 and R_2 here than in Example 5.11 introduce a low input impedance, loading the preceding stage. We compute the exact input impedance of this circuit in Section 5.3.1.

Exercise

Repeat the above example if V_{RE} is limited to 100 mV.

5.2.4 Self-Biased Stage

Another biasing scheme commonly used in discrete and integrated circuits is shown in Fig. 5.22. Called "self-biased" because the base current and voltage are provided from the collector, this stage exhibits many interesting and useful attributes.

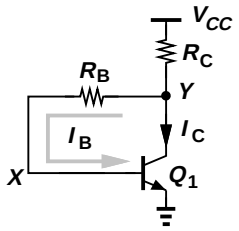


Figure 5.22 Self-biased stage.

Let us begin the analysis of the circuit with the observation that the base voltage is always *lower* than the collector voltage: $V_X = V_Y - I_B R_B$. A result of self-biasing, this important property guarantees that Q_1 operates in the active mode regardless of device and circuit parameters. For example, if R_C increases indefinitely, Q_1 remains in the active region, a critical advantage over the circuit of Fig. 5.21.

We now determine the collector bias current by assuming $I_B \ll I_C$; i.e., R_C carries a current equal to I_C, thereby yielding

$$V_Y = V_{CC} - R_C I_C. \tag{5.75}$$

Also,

$$V_Y = R_B I_B + V_{BE} \tag{5.76}$$

$$= \frac{R_B I_C}{\beta} + V_{BE}. \tag{5.77}$$

Equating the right hand sides of (5.75) and (5.77) gives

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \dfrac{R_B}{\beta}}. \tag{5.78}$$

As usual, we begin with an initial guess for V_{BE}, compute I_C, and utilize $V_{BE} = V_T \ln(I_C/I_S)$ to improve the accuracy of our calculations.

Example 5.13

Determine the collector current and voltage of Q_1 in Fig. 5.22 if $R_C = 1\ \text{k}\Omega$, $R_B = 10\ \text{k}\Omega$, $V_{CC} = 2.5$ V, $I_S = 5 \times 10^{-17}$ A, and $\beta = 100$. Repeat the calculations for $R_C = 2\ \text{k}\Omega$.

Solution

Assuming $V_{BE} = 0.8$ V, we have from (5.78):

$$I_C = 1.545 \text{ mA}, \tag{5.79}$$

and hence $V_{BE} = V_T \ln(I_C/I_S) = 807.6$ mV, concluding that the initial guess for V_{BE} and the value of I_C given by it are reasonably accurate. We also note that $R_B I_B = 154.5$ mV and $V_Y = R_B I_B + V_{BE} \approx 0.955$ V.

If $R_C = 2$ kΩ, then with $V_{BE} = 0.8$ V, Eq. (5.78) gives

$$I_C = 0.810 \text{ mA}. \tag{5.80}$$

To check the validity of the initial guess, we write $V_{BE} = V_T \ln(I_C/I_S) = 791$ mV. Compared with $V_{CC} - V_{BE}$ in the numerator of (5.78), the 9-mV error is negligible and the value of I_C in (5.80) is acceptable. Since $R_B I_B = 81$ mV, $V_Y \approx 0.881$ V.

Exercise

What happens if the base resistance is doubled?

Equation (5.78) and the above example suggest two important guidelines for the design of the self-biased stage: (1) $V_{CC} - V_{BE}$ must be much greater than the uncertainties in the value of V_{BE}; (2) R_C must be much greater than R_B/β to lower sensitivity to β. In fact, if $R_C \gg R_B/\beta$, then

$$I_C \approx \frac{V_{CC} - V_{BE}}{R_C}, \tag{5.81}$$

and $V_Y = V_{CC} - I_C R_C \approx V_{BE}$. This result serves as a quick estimate of the transistor bias conditions.

Design Procedure Equation (5.78) together with the condition $R_C \gg R_B/\beta$ provides the basic expressions for the design of the circuit. With the required value of I_C known from small-signal considerations, we choose $R_C = 10R_B/\beta$ and rewrite (5.78) as

$$I_C = \frac{V_{CC} - V_{BE}}{1.1R_C}, \tag{5.82}$$

where $V_{BE} = V_T \ln(I_C/I_S)$. That is,

$$R_C = \frac{V_{CC} - V_{BE}}{1.1I_C} \tag{5.83}$$

$$R_B = \frac{\beta R_C}{10}. \tag{5.84}$$

The choice of R_B also depends on small-signal requirements and may deviate from this value, but it must remain substantially lower than βR_C.

Example 5.14

Design the self-biased stage of Fig. 5.22 for $g_m = 1/(13\ \Omega)$ and $V_{CC} = 1.8$ V. Assume $I_S = 5 \times 10^{-16}$ A and $\beta = 100$.

Solution

Since $g_m = I_C/V_T = 1/(13\,\Omega)$, we have $I_C = 2$ mA, $V_{BE} = 754$ mV, and

$$R_C \approx \frac{V_{CC} - V_{BE}}{1.1 I_C} \tag{5.85}$$

$$\approx 475\ \Omega. \tag{5.86}$$

Also,

$$R_B = \frac{\beta R_C}{10} \tag{5.87}$$

$$= 4.75\ \text{k}\Omega. \tag{5.88}$$

Note that $R_B I_B = 95$ mV, yielding a collector voltage of $754\ \text{mV} + 95\ \text{mV} = 849$ mV.

Exercise

Repeat the above design with a supply voltage of 2.5 V.

Figure 5.23 summarizes the biasing principles studied in this section.

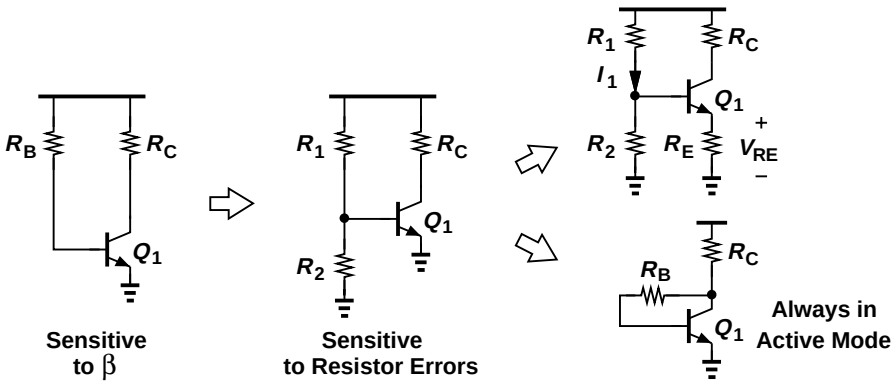


Figure 5.23 Summary of biasing techniques.

5.2.5 Biasing of PNP Transistors

The dc bias topologies studied thus far incorporate npn transistors. Circuits using pnp devices follow the same analysis and design procedures while requiring attention to voltage and current polarities. We illustrate these points with the aid of some examples.

Example 5.15

Calculate the collector and voltage of Q_1 in the circuit of Fig. 5.24 and determine the maximum allowable value of R_C for operation in the active mode.

Solution

The topology is the same as that in Fig. 5.13 and we have,

$$I_B R_B + V_{EB} = V_{CC}. \tag{5.89}$$

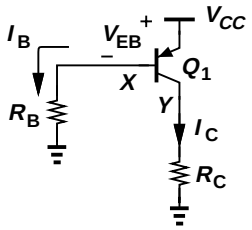


Figure 5.24 Simple biasing of *pnp* stage.

That is,

$$I_B = \frac{V_{CC} - V_{EB}}{R_B} \tag{5.90}$$

and

$$I_C = \beta \frac{V_{CC} - V_{EB}}{R_B}. \tag{5.91}$$

The circuit suffers from sensitivity to β.

If R_C is increased, V_Y rises, thus approaching V_X ($= V_{CC} - V_{EB}$) and bringing Q_1 closer to saturation. The transistor enters saturation at $V_Y = V_X$, i.e.,

$$I_C R_{C,max} = V_{CC} - V_{EB} \tag{5.92}$$

and hence

$$R_{C,max} = \frac{V_{CC} - V_{EB}}{I_C} \tag{5.93}$$

$$= \frac{R_B}{\beta}. \tag{5.94}$$

From another perspective, since $V_X = I_B R_B$ and $V_Y = I_C R_C$, we have $I_B R_B = I_C R_{C,max}$ as the condition for edge of saturation, obtaining $R_B = \beta R_{C,max}$.

Exercise

For a given R_C, what value of R_B places the device at the edge of saturation?

Example 5.16

Determine the collector current and voltage of Q_1 in the circuit of Fig. 5.25(a).

Solution

As a general case, we assume I_B is significant and construct the Thevenin equivalent of the voltage divider as depicted in Fig. 5.25(b):

$$V_{Thev} = \frac{R_1}{R_1 + R_2} V_{CC} \tag{5.95}$$

$$R_{Thev} = R_1 || R_2. \tag{5.96}$$

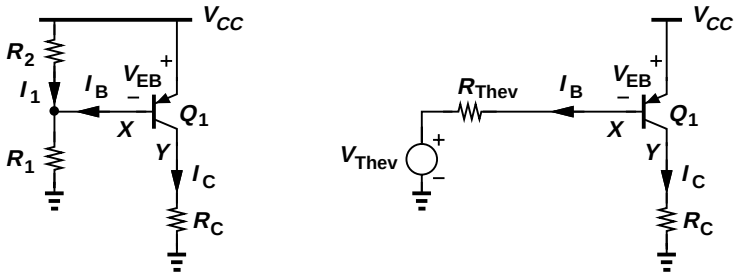


Figure 5.25 (a) PNP stage with resistive divider biasing, (b) Thevenin equivalent of divider and V_{CC}.

Adding the voltage drop across R_{Thev} and V_{EB} to V_{Thev} yields

$$V_{Thev} + I_B R_{Thev} + V_{EB} = V_{CC}; \tag{5.97}$$

that is,

$$I_B = \frac{V_{CC} - V_{Thev} - V_{EB}}{R_{Thev}} \tag{5.98}$$

$$= \frac{\dfrac{R_2}{R_1 + R_2} V_{CC} - V_{EB}}{R_{Thev}}. \tag{5.99}$$

It follows that

$$I_C = \beta \frac{\dfrac{R_2}{R_1 + R_2} V_{CC} - V_{EB}}{R_{Thev}}. \tag{5.100}$$

As in Example 5.9, some iteration between I_C and V_{EB} may be necessary.

Equation (5.100) indicates that if I_B is significant, then the transistor bias heavily depends on β. On the other hand, if $I_B \ll I_1$, we equate the voltage drop across R_2 to V_{EB}, thereby obtaining the collector current:

$$\frac{R_2}{R_1 + R_2} V_{CC} = V_{EB} \tag{5.101}$$

$$I_C = I_S \exp\left(\frac{R_2}{R_1 + R_2} \frac{V_{CC}}{V_T}\right). \tag{5.102}$$

Note that this result is identical to Eq. (5.30).

Exercise

What is the maximum value of R_C is Q_1 must remain in soft saturation?

Example 5.17

Assuming a negligible base current, calculate the collector current and voltage of Q_1 in the

circuit of Fig. 5.26. What is the maximum allowable value of R_C for Q_1 to operate in the forward active region?

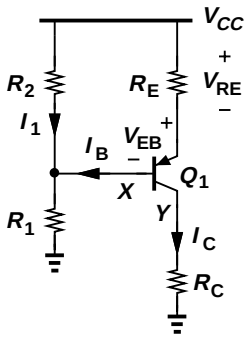


Figure 5.26 PNP stage with degeneration resistor.

Solution

With $I_B \ll I_1$, we have $V_X = V_{CC}R_1/(R_1 + R_2)$. Adding to V_X the emitter-base voltage and the drop across R_E, we obtain

$$V_X + V_{EB} + R_E I_E = V_{CC} \tag{5.103}$$

and hence

$$I_E = \frac{1}{R_E}\left(\frac{R_2}{R_1 + R_2}V_{CC} - V_{EB}\right). \tag{5.104}$$

Using $I_C \approx I_E$, we can compute a new value for V_{EB} and iterate if necessary. Also, with $I_B = I_C/\beta$, we can verify the assumption $I_B \ll I_1$.

In arriving at (5.104), we have written a KVL from V_{CC} to ground, Eq. (5.103). But a more straightforward approach is to recognize that the voltage drop across R_2 is equal to $V_{EB} + I_E R_E$, i.e.,

$$V_{CC}\frac{R_2}{R_1 + R_2} = V_{EB} + I_E R_E, \tag{5.105}$$

which yields the same result as in (5.104).

The maximum allowable value of R_C is obtained by equating the base and collector voltages:

$$V_{CC}\frac{R_1}{R_1 + R_2} = R_{C,max} I_C \tag{5.106}$$

$$\approx \frac{R_{C,max}}{R_E}\left(\frac{R_2}{R_1 + R_2}V_{CC} - V_{EB}\right). \tag{5.107}$$

It follows that

$$R_{C,max} = R_E V_{CC}\frac{R_1}{R_1 + R_2} \cdot \frac{1}{\dfrac{R_2}{R_1 + R_2}V_{CC} - V_{EB}}. \tag{5.108}$$

Exercise

Repeat the above example if $R_2 = \infty$.

Example 5.18

Determine the collector current and voltage of Q_1 in the self-biased circuit of Fig. 5.27.

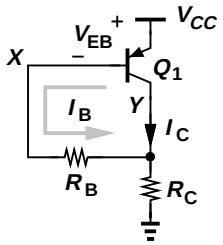


Figure 5.27 Self-biased *pnp* stage.

Solution

We must write a KVL from V_{CC} through the emitter-base junction of Q_1, R_B, and R_C to ground. Since $\beta \gg 1$ and hence $I_C \gg I_B$, R_C carries a current approximately equal to I_C, creating $V_Y = R_C I_C$. Moreover, $V_X = R_B I_B + V_Y = R_B I_B + R_C I_C$, yielding

$$V_{CC} = V_{EB} + V_X \tag{5.109}$$

$$= V_{EB} + R_B I_B + I_C R_C \tag{5.110}$$

$$= V_{EB} + \left(\frac{R_B}{\beta} + R_C \right) I_C. \tag{5.111}$$

Thus,

$$I_C = \frac{V_{CC} - V_{EB}}{\dfrac{R_B}{\beta} + R_C}, \tag{5.112}$$

a result similar to Eq. (5.78). As usual, we begin with a guess for V_{EB}, compute I_C, and determine a new value for V_{EB}, etc. Note that, since the base is *higher* than the collector voltage, Q_1 always remains in the active mode.

Exercise

How far is Q_1 from saturation?

5.3 Bipolar Amplifier Topologies

Following our detailed study of biasing, we can now delve into different amplifier topologies and examine their small-signal properties.[6]

Since the bipolar transistor contains three terminals, we may surmise that three possibilities exist for applying the input signal to the device, as conceptually illustrated in Figs. 5.28(a)-(c). Similarly, the output signal can be sensed from any of the terminals (with respect to ground) [Figs. 5.28(d)-(f)], leading to nine possible combinations of input and output networks and hence nine amplifier topologies.

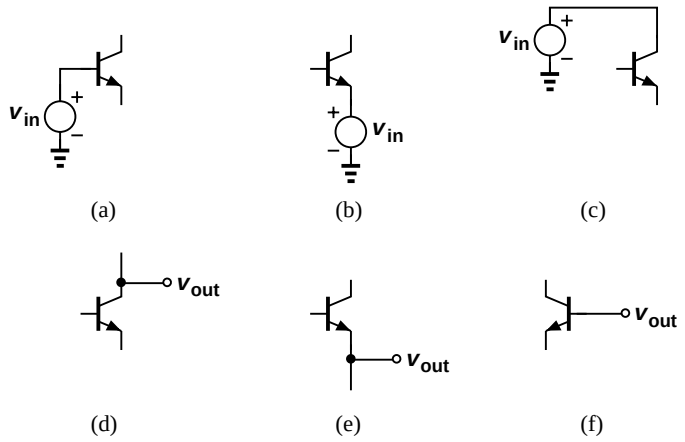


Figure 5.28 Possible input and output connections to a bipolar transistor.

However, as seen in Chapter 4, bipolar transistors operating in the active mode respond to base-emitter voltage variations by varying their collector current. This property rules out the input connection shown in Fig. 5.28(c) because here V_{in} does not affect the base or emitter voltages. Also, the topology in Fig. 5.28(f) proves of no value as V_{out} is not a function of the collector current. The number of possibilities therefore falls to four. But we note that the input and output connections in Figs. 5.28(b) and (e) remain incompatible because V_{out} would be sensed at the *input* node (the emitter) and the circuit would provide no function.

The above observations reveal three possible amplifier topologies. We study each carefully, seeking to compute its gain and input and output impedances. In all cases, the bipolar transistors operate in the active mode. The reader is encouraged to review Examples (5.2)-(5.4) and the three resulting rules illustrated in Fig. 5.7 before proceeding further.

5.3.1 Common-Emitter Topology

Our initial thoughts in Section 4.1 pointed to the circuit of Fig. 4.1(b) and hence the topology of Fig. 4.25 as an amplifier. If the input signal is applied to the base [Fig. 5.28(a)] and the output signal is sensed at the collector [Fig. 5.28(d)], the circuit is called a "common-emitter" (CE) stage (Fig. 5.29). We have encountered and analyzed this circuit in different contexts without giving it a name. The term "common-emitter" is used because the emitter terminal is grounded and hence appears *in common* to the input and output ports. Nevertheless, we identify the stage based on the input and output connections (to the base and from the collector, respectively) so as to avoid confusion in more complex topologies.

[6] While beyond the scope of this book, the large-signal behavior of amplifiers also becomes important in many applications.

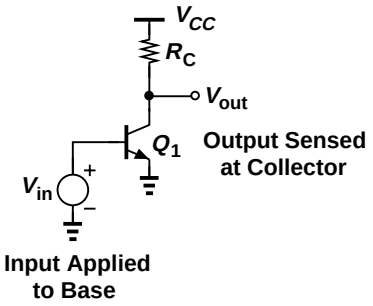


Figure 5.29 Common-emitter stage.

We deal with the CE amplifier in two phases: (a) analysis of the CE core to understand its fundamental properties, and (b) analysis of the CE stage including the bias circuitry as a more realistic case.

Analysis of CE Core Recall from the definition of transconductance in Section 4.4.3 that a small increment of ΔV applied to the base of Q_1 in Fig. 5.29 increases the collector current by $g_m \Delta V$ and hence the voltage drop across R_C by $g_m \Delta V R_C$. In order to examine the amplifying properties of the CE stage, we construct the small-signal equivalent of the circuit, shown in Fig. 5.30. As explained in Chapter 4, the supply voltage node, V_{CC}, acts as an ac ground because its value remains constant with time. We neglect the Early effect for now.

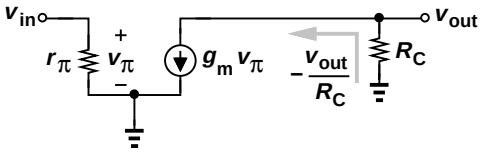


Figure 5.30 Small-signal model of CE stage.

Let us first compute the small-signal voltage gain $A_v = v_{out}/v_{in}$. Beginning from the output port and writing a KCL at the collector node, we have

$$-\frac{v_{out}}{R_C} = g_m v_\pi, \tag{5.113}$$

and $v_\pi = v_{in}$. It follows that

$$A_v = -g_m R_C. \tag{5.114}$$

Equation (5.114) embodies two interesting and important properties of the CE stage. First, the small-signal gain is *negative* because raising the base voltage and hence the collector current in Fig. 5.29 *lowers* V_{out}. Second, A_v is proportional to g_m (i.e., the collector bias current) and the collector resistor, R_C.

Interestingly, the voltage gain of the stage is limited by the supply voltage. A higher collector bias current or a larger R_C demands a greater voltage drop across R_C, but this drop cannot exceed V_{CC}. In fact, denoting the dc drop across R_C with V_{RC} and writing $g_m = I_C/V_T$, we express (5.114) as

$$|A_v| = \frac{I_C R_C}{V_T} \tag{5.115}$$

$$= \frac{V_{RC}}{V_T}. \tag{5.116}$$

Since $V_{RC} < V_{CC}$,

$$|A_v| < \frac{V_{CC}}{V_T}. \tag{5.117}$$

Furthermore, the transistor itself requires a minimum collector-emitter voltage of about V_{BE} to remain in the active region, lowering the limit to

$$|A_v| < \frac{V_{CC} - V_{BE}}{V_T}. \tag{5.118}$$

Example 5.19

Design a CE core with $V_{CC} = 1.8$ V and a power budget, P, of 1 mW while achieving maximum voltage gain.

Solution

Since $P = I_C \cdot V_{CC} = 1$ mW, we have $I_C = 0.556$ mA. The value of R_C that places Q_1 at the edge of saturation is given by

$$V_{CC} - R_C I_C = V_{BE}, \tag{5.119}$$

which, along with $V_{BE} \approx 800$ mV, yields

$$R_C \leq \frac{V_{CC} - V_{BE}}{I_C} \tag{5.120}$$

$$\leq 1.8\ \text{k}\Omega. \tag{5.121}$$

The voltage gain is therefore equal to

$$A_v = -g_m R_C \tag{5.122}$$

$$= -38.5. \tag{5.123}$$

Under this condition, an input signal drives the transistor into saturation. As illustrated in Fig. 5.31(a), a 2-mV_{pp} input results in a 77-mV_{pp} output, forward-biasing the base-collector junction for half of each cycle. Nevertheless, so long as Q_1 remains in soft saturation ($V_{BC} > 400$ mV), the circuit amplifies properly.

A more aggressive design may allow Q_1 to operate in soft saturation, e.g., $V_{CE} \approx 400$ mV and hence

$$R_C \leq \frac{V_{CC} - 400\ \text{mV}}{I_C} \tag{5.124}$$

$$\leq 2.52\ \text{k}\Omega. \tag{5.125}$$

In this case, the maximum voltage gain is given by

$$A_v = -53.9. \tag{5.126}$$

Of course, the circuit can now tolerate only very small voltage swings at the output. For example, a 2-mV_{pp} input signal gives rise to a 107.8-mV_{pp} output, driving Q_1 into heavy saturation [Fig.

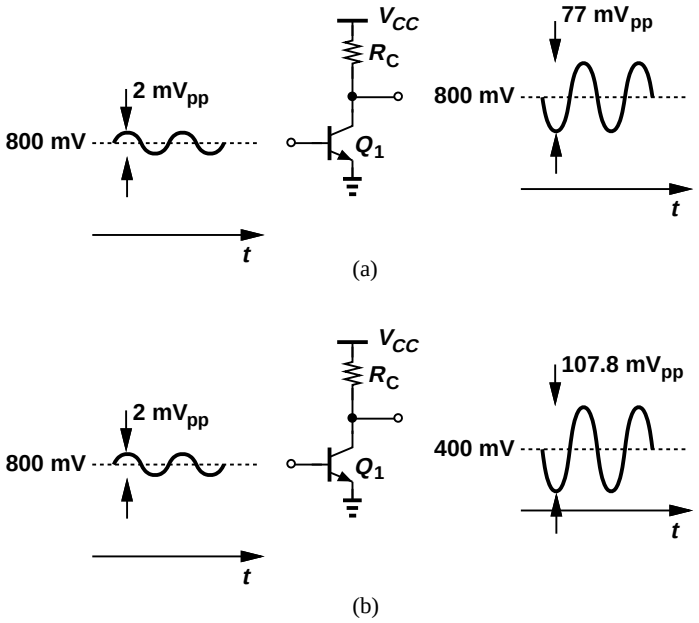


Figure 5.31 CE stage (a) with some signal levels, (b) in saturation.

5.31(b)]. We say the circuit suffers from a trade-off between voltage gain and voltage "headroom."

Exercise

Repeat the above example if $V_{CC} = 2.5$ V and compare the results.

Let us now calculate the I/O impedances of the CE stage. Using the equivalent circuit depicted in Fig. 5.32(a), we write

$$R_{in} = \frac{v_X}{i_X} \tag{5.127}$$

$$= r_\pi . \tag{5.128}$$

Thus, the input impedance is simply equal to $\beta/g_m = \beta V_T/I_C$ and decreases as the collector bias increases.

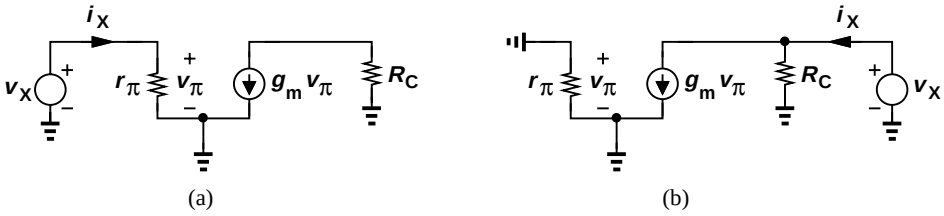


Figure 5.32 (a) Input and (b) output impedance calculation of CE stage.

The output impedance is obtained from Fig. 5.32(b), where the input voltage source is set to zero (replaced with a short). Since $v_\pi = 0$, the dependent current source also vanishes, leaving

R_C as the only component seen by v_X. In other words,

$$R_{out} = \frac{v_X}{i_X} \tag{5.129}$$

$$= R_C. \tag{5.130}$$

The output impedance therefore trades with the voltage gain, $-g_m R_C$.

Figure 5.33 summarizes the trade-offs in the performance of the CE topology along with the parameters that create such trade-offs. For example, for a given value of output impedance, R_C is fixed and the voltage gain can be increased by increasing I_C, thereby lowering both the voltage headroom and the input impedance.

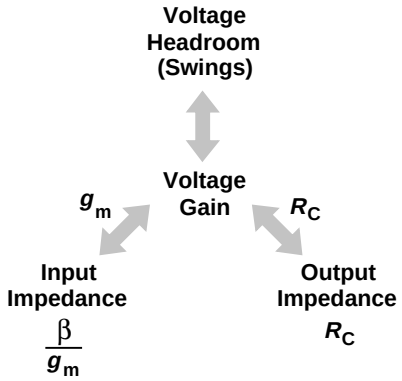


Figure 5.33 CE stage trade-offs.

Example 5.20

A CE stage must achieve an input impedance of R_{in} and an output impedance of R_{out}. What is the voltage gain of the circuit?

Solution

Since $R_{in} = r_\pi = \beta/g_m$ and $R_{out} = R_C$, we have

$$A_v = -g_m R_C \tag{5.131}$$

$$= -\beta \frac{R_{out}}{R_{in}}. \tag{5.132}$$

Interestingly, if the I/O impedances are specified, then the voltage gain is automatically set. We will develop other circuits in this book that avoid this "coupling" of design specifications.

Exercise

What happens to this result if the supply voltage is halved?

Inclusion of Early Effect Equation (5.114) suggests that the voltage gain of the CE stage can be increased indefinitely if $R_C \to \infty$ while g_m remains constant. Mentioned in Section 4.4.5, this trend appears valid if V_{CC} is also raised to ensure the transistor remains in the active mode. From an intuitive point of view, a given change in the input voltage and hence the collector current gives rise to an increasingly larger output swing as R_C increases.

In reality, however, the Early effect limits the voltage gain even if R_C approaches infinity. Since achieving a high gain proves critical in circuits such as operational amplifiers, we must reexamine the above derivations in the presence of the Early effect.

Figure 5.34 depicts the small-signal equivalent circuit of the CE stage including the transistor output resistance. Note that r_O appears in parallel with R_C, allowing us to rewrite (5.114) as

$$A_v = -g_m(R_C||r_O). \tag{5.133}$$

We also recognize that the input impedance remains equal to r_π whereas the output impedance falls to

$$R_{out} = R_C||r_O. \tag{5.134}$$

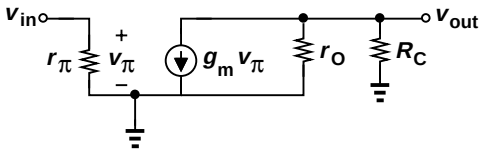


Figure 5.34 CE stage including Early effect.

Example 5.21

The circuit of Fig. 5.29 is biased with a collector current of 1 mA and $R_C = 1\ \text{k}\Omega$. If $\beta = 100$ and $V_A = 10$ V, determine the small-signal voltage gain and the I/O impedances.

Solution

We have

$$g_m = \frac{I_C}{V_T} \tag{5.135}$$

$$= (26\ \Omega)^{-1} \tag{5.136}$$

and

$$r_O = \frac{V_A}{I_C} \tag{5.137}$$

$$= 10\ \text{k}\Omega. \tag{5.138}$$

Thus,

$$A_v = -g_m(R_C||r_O) \tag{5.139}$$

$$\approx 35. \tag{5.140}$$

(As a comparison, if $V_A = \infty$, then $A_v \approx 38$.) For the I/O impedances, we write

$$R_{in} = r_\pi \tag{5.141}$$

$$= \frac{\beta}{g_m} \tag{5.142}$$

$$= 2.6\ \text{k}\Omega \tag{5.143}$$

and

$$R_{out} = R_C||r_O \tag{5.144}$$

$$= 0.91\ \text{k}\Omega. \tag{5.145}$$

Exercise

Calculate the gain if $V_A = 5$ V.

Let us determine the gain of a CE stage as $R_C \to \infty$. Equation (5.133) gives

$$A_v = -g_m r_O. \tag{5.146}$$

Called the "intrinsic gain" of the transistor to emphasize that no external device loads the circuit, $g_m r_O$ represents the *maximum* voltage gain provided by a single transistor, playing a fundamental role in high-gain amplifiers.

We now substitute $g_m = I_C/V_T$ and $r_O = V_A/I_C$ in Eq. (5.133), thereby arriving at

$$|A_v| = \frac{V_A}{V_T}. \tag{5.147}$$

Interestingly, the intrinsic gain of a bipolar transistor is independent of the bias current. In modern integrated bipolar transistors, V_A falls in the vicinity of 5 V, yielding a gain of nearly 200.[7] In this book, we assume $g_m r_O \gg 1$ (and hence $r_O \gg 1/g_m$) for all transistors.

Another parameter of the CE stage that may prove relevant in some applications is the "current gain," defined as

$$A_I = \frac{i_{out}}{i_{in}}, \tag{5.148}$$

where i_{out} denotes the current delivered to the load and i_{in} the current flowing to the input. We rarely deal with this parameter for voltage amplifiers, but note that $A_I = \beta$ for the stage shown in Fig. 5.29 because the entire collector current is delivered to R_C.

CE Stage With Emitter Degeneration In many applications, the CE core of Fig. 5.29 is modified as shown in Fig. 5.35(a), where a resistor R_E appears in series with the emitter. Called "emitter degeneration," this technique improves the "linearity" of the circuit and provides many other interesting properties that are studied in more advanced courses.

As with the CE core, we intend to determine the voltage gain and I/O impedances of the circuit, assuming Q_1 is biased properly. Before delving into a detailed analysis, it is instructive to make some qualitative observations. Suppose the input signal raises the base voltage by ΔV [Fig. 5.35(b)]. If R_E were zero, then the base-emitter voltage would also increase by ΔV, producing a collector current change of $g_m \Delta V$. But with $R_E \neq 0$, some fraction of ΔV appears across R_E, thus leaving a voltage change across the BE junction that is *less* than ΔV. Consequently, the collector current change is also less than $g_m \Delta V$. We therefore expect that the voltage gain of

[7] But other second-order effects limit the actual gain to about 50.

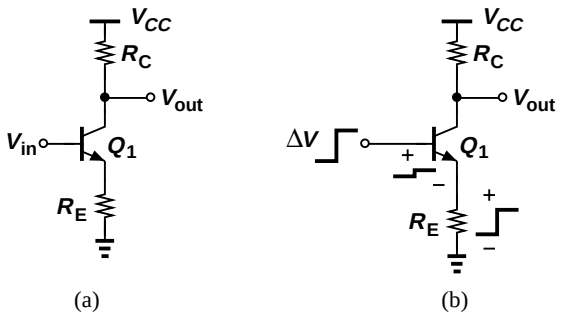


Figure 5.35 (a) CE stage with degeneration, (b) effect of input voltage change.

the degenerated stage is *lower* than that of the CE core with no degeneration. While undesirable, the reduction in gain is incurred to improve other aspects of the performance.

How about the input impedance? Since the collector current change is less than $g_m \Delta V$, the base current also changes by less than $g_m \Delta V/\beta$, yielding an input impedance *greater* than $\beta/g_m = r_\pi$. Thus, emitter degeneration *increases* the input impedance of the CE stage, a desirable property. A common mistake is to conclude that $R_{in} = r_\pi + R_E$, but as explained below, $R_{in} = r_\pi + (\beta + 1)R_E$.

We now quantify the foregoing observations by analyzing the small-signal behavior of the circuit. Depicted in Fig. 5.36 is the small-signal equivalent circuit, where V_{CC} is replaced with an ac ground and the Early effect is neglected. Note that v_π appears across r_π and *not* from the base to ground. To determine v_{out}/v_{in}, we first write a KCL at the output node,

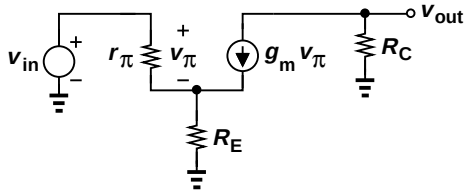


Figure 5.36 Small-signal model of CE stage with emitter degeneration.

$$g_m v_\pi = -\frac{v_{out}}{R_C}, \tag{5.149}$$

obtaining

$$v_\pi = -\frac{v_{out}}{g_m R_C}. \tag{5.150}$$

We also recognize that two currents flow through R_E: one originating from r_π equal to v_π/r_π and another equal to $g_m v_\pi$. Thus, the voltage drop across R_E is given by

$$v_{RE} = \left(\frac{v_\pi}{r_\pi} + g_m v_\pi\right) R_E. \tag{5.151}$$

Since the voltage drop across r_π and R_E must add up to v_{in}, we have

$$v_{in} = v_\pi + v_{RE} \tag{5.152}$$

$$= v_\pi + \left(\frac{v_\pi}{r_\pi} + g_m v_\pi\right) R_E \tag{5.153}$$

$$= v_\pi \left[1 + \left(\frac{1}{r_\pi} + g_m\right) R_E\right]. \tag{5.154}$$

Substituting for v_π from (5.150) and rearranging the terms, we arrive at

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_C}{1 + \left(\frac{1}{r_\pi} + g_m\right) R_E}. \tag{5.155}$$

As predicted earlier, the magnitude of the voltage gain is lower than $g_m R_C$ for $R_E \neq 0$. With $\beta \gg 1$, we can assume $g_m \gg 1/r_\pi$ and hence

$$A_v = -\frac{g_m R_C}{1 + g_m R_E}. \tag{5.156}$$

Thus, the gain falls by a factor of $1 + g_m R_E$.

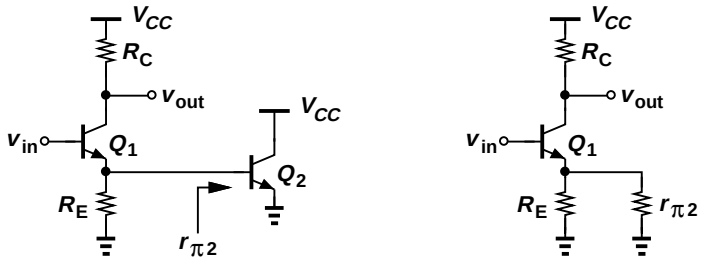
To arrive at an interesting interpretation of Eq. (5.156), we divide the numerator and denominator by g_m,

$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}. \tag{5.157}$$

It is helpful to memorize this result as "the gain of the degenerated CE stage is equal to the total load resistance seen at the collector (to ground) divided by $1/g_m$ plus the total resistance placed in series with the emitter." (In verbal descriptions, we often ignore the negative sign in the gain, with the understanding that it must be included.) This and similar interpretations throughout this book greatly simplify the analysis of amplifiers—often obviating the need for drawing small-signal circuits.

Example 5.22

Determine the voltage gain of the stage shown in Fig. 5.37(a).



(a) (b)

Figure 5.37 (a) CE stage example, (b) simplified circuit.

Solution

We identify the circuit as a CE stage because the input is applied to the base of Q_1 and the output is sensed at its collector. This transistor is degenerated by two devices: R_E and the base-emitter junction of Q_2. The latter exhibits an impedance of $r_{\pi 2}$ (as illustrated in Fig. 5.7), leading to the simplified model depicted in Fig. 5.37(b). The total resistance placed in series with the emitter is

therefore equal to $R_E||r_{\pi 2}$, yielding

$$A_v = -\frac{R_C}{\dfrac{1}{g_{m1}} + R_E||r_{\pi 2}}. \tag{5.158}$$

Without the above observations, we would need to draw the small-signal model of both Q_1 and Q_2 and solve a system of several equations.

Exercise

Repeat the above example if a resistor is placed in series with the emitter of Q_2.

Example 5.23

Calculate the voltage gain of the circuit in Fig. 5.38(a).

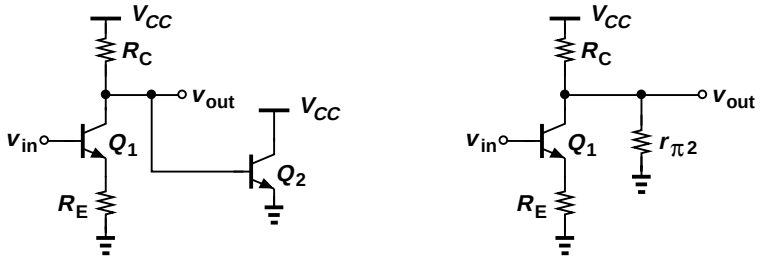


Figure 5.38 (a) CE stage example, (b) simplified circuit.

Solution

The topology is a CE stage degenerated by R_E, but the load resistance between the collector of Q_1 and ac ground consists of R_C and the base-emitter junction of Q_2. Modeling the latter by $r_{\pi 2}$, we reduce the circuit to that shown in Fig. 5.38(b), where the total load resistance seen at the collector of Q_1 is equal to $R_C||r_{\pi 2}$. The voltage gain is thus given by

$$A_v = -\frac{R_C||r_{\pi 2}}{\dfrac{1}{g_{m1}} + R_E}. \tag{5.159}$$

Exercise

Repeat the above example if a resistor is placed in series with the emitter of Q_2.

To compute the input impedance of the degenerated CE stage, we redraw the small-signal model as in Fig. 5.39(a) and calculate v_X/i_X. Since $v_\pi = r_\pi i_X$, the current flowing through R_E is equal to $i_X + g_m r_\pi i_X = (1+\beta)i_X$, creating a voltage drop of $R_E(1+\beta)i_X$. Summing v_π and v_{RE} and equating the result to v_X, we have

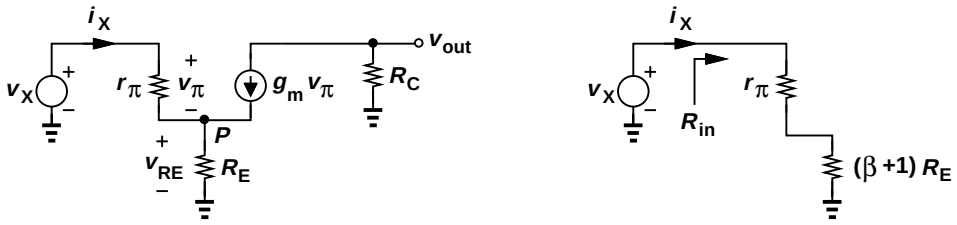


Figure 5.39 (a) Input impedance of degenerated CE stage, (b) equivalent circuit.

$$v_X = r_\pi i_X + R_E(1+\beta)i_X, \tag{5.160}$$

and hence

$$R_{in} = \frac{v_X}{i_X} \tag{5.161}$$

$$= r_\pi + (\beta+1)R_E. \tag{5.162}$$

As predicted by our qualitative reasoning, emitter degeneration increases the input impedance [Fig. 5.39(b)].

Why is R_{in} not simply equal to $r_\pi + R_E$? This would hold only if r_π and R_E were exactly in series, i.e., if the two carried equal currents, but in the circuit of Fig. 5.39(a), the collector current, $g_m v_\pi$, also flows into node P.

Does the factor $\beta + 1$ bear any intuitive meaning? We observe that the flow of both base and collector currents through R_E results in a large voltage drop, $(\beta+1)i_X R_E$, even though the current drawn from v_X is merely i_X. In other words, the test voltage source, v_X, supplies a current of only i_X while producing a voltage drop of $(\beta+1)i_X R_E$ across R_E—as if i_X flows through a resistor equal to $(\beta+1)R_E$.

The above observation is articulated as follows: any impedance tied between the emitter and ground is multiplied by $\beta + 1$ when "seen from the base." The expression "seen from the base" means the impedance measured between the base and ground.

We also calculate the output impedance of the stage with the aid of the equivalent shown in Fig. 5.40, where the input voltage is set to zero. Equation (5.153) applies to this circuit as well:

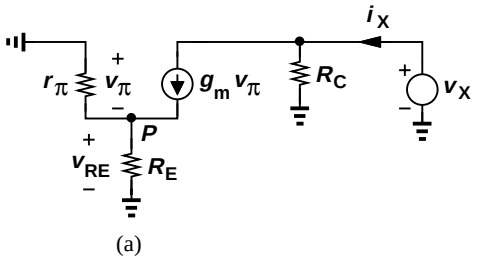


Figure 5.40 Output impedance of degenerated stage.

$$v_{in} = 0 = v_\pi + \left(\frac{v_\pi}{r_\pi} + g_m v_\pi\right) R_E, \tag{5.163}$$

yielding $v_\pi = 0$ and hence $g_m v_\pi = 0$. Thus, all of i_X flows through R_C, and

$$R_{out} = \frac{v_X}{i_X} \tag{5.164}$$

$$= R_C, \tag{5.165}$$

revealing that emitter degeneration does not alter the output impedance if the Early effect is neglected.

Example 5.24

A CE stage is biased at a collector current of 1 mA. If the circuit provides a voltage gain of 20 with no emitter degeneration and 10 with degeneration, determine R_C, R_E, and the I/O impedances. Assume $\beta = 100$.

Solution

For $A_v = 20$ in the absence of degeneration, we require

$$g_m R_C = 20, \tag{5.166}$$

which, together with $g_m = I_C/V_T = (26\,\Omega)^{-1}$, yields

$$R_C = 520\,\Omega. \tag{5.167}$$

Since degeneration lowers the gain by a factor of two,

$$1 + g_m R_E = 2, \tag{5.168}$$

i.e.,

$$R_E = \frac{1}{g_m} \tag{5.169}$$

$$= 26\,\Omega. \tag{5.170}$$

The input impedance is given by

$$R_{in} = r_\pi + (\beta + 1)R_E \tag{5.171}$$

$$= \frac{\beta}{g_m} + (\beta + 1)R_E \tag{5.172}$$

$$\approx 2r_\pi \tag{5.173}$$

because $\beta \gg 1$ and $R_E = 1/g_m$ in this example. Thus, $R_{in} = 5200\,\Omega$. Finally,

$$R_{out} = R_C \tag{5.174}$$

$$= 520\,\Omega. \tag{5.175}$$

Exercise

What bias current would result in a gain of 5 with such emitter and collector resistor values?

Example 5.25

Compute the voltage gain and I/O impedances of the circuit depicted in Fig. 5.41. Assume a very large value for C_1.

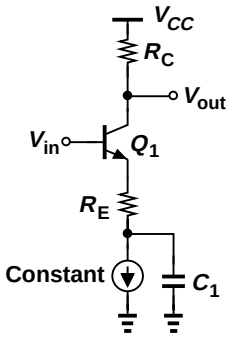


Figure 5.41 CE stage example.

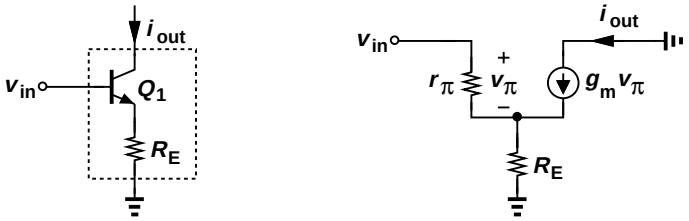
Solution

If C_1 is very large, it acts as a short circuit for the signal frequencies of interest. Also, the constant current source is replaced with an open circuit in the small-signal equivalent circuit. Thus, the stage reduces to that in Fig. 5.35(a) and Eqs. (5.157), (5.162), (5.165) apply.

Exercise

Repeat the above example if we tie another capacitor from the base to ground.

The degenerated CE stage can be analyzed from a different perspective to provide more insight. Let us place the transistor and the emitter resistor in a black box having still three terminals [Fig. 5.42(a)]. For small-signal operation, we can view the box as a new transistor (or "active" device) and model its behavior by new values of transconductance and impedances. Denoted by G_m to avoid confusion with g_m of Q_1, the equivalent transconductance is obtained from Fig. 5.42(b). Since Eq. (5.154) still holds, we have



(a) (b)

Figure 5.42 (a) Degenerated bipolar transistor viewed as a black box, (b) small-signal equivalent.

$$i_{out} = g_m v_\pi \tag{5.176}$$

$$= g_m \frac{v_{in}}{1 + (r_\pi^{-1} + g_m) R_E}, \tag{5.177}$$

and hence

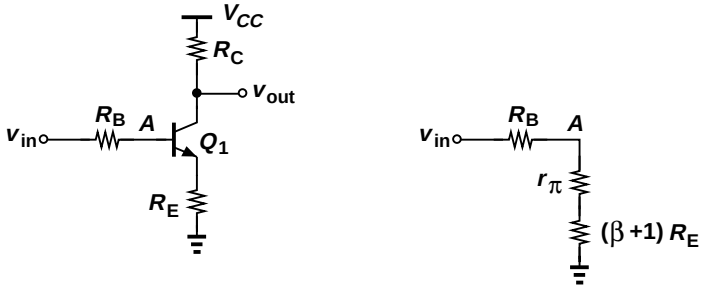
$$G_m = \frac{i_{out}}{v_{in}} \tag{5.178}$$

$$\approx \frac{g_m}{1+g_m R_E}. \tag{5.179}$$

For example, the voltage gain of the stage with a load resistance of R_D is given by $-G_m R_D$.

An interesting property of the degenerated CE stage is that its voltage gain becomes relatively independent of the transistor transconductance and hence bias current if $g_m R_E \gg 1$. From Eq. (5.157), we note that $A_v \to -R_C/R_E$ under this condition. As studied in Problem 40, this trend in fact represents the "linearizing" effect of emitter degeneration.

As a more general case, we now consider a degenerated CE stage containing a resistance in series with the base [Fig. 5.43(a)]. As seen below, R_B only *degrades* the performance of the circuit, but often proves inevitable. For example, R_B may represent the output resistance of a microphone connected to the input of the amplifier.



(a) (b)

Figure 5.43 (a) CE stage with base resistance, (b) equivalent circuit.

To analyze the small-signal behavior of this stage, we can adopt one of two approaches: (a) draw the small-signal model of the entire circuit and solve the resulting equations, or (b) recognize that the signal at node A is simply an attenuated version of v_{in} and write

$$\frac{v_{out}}{v_{in}} = \frac{v_A}{v_{in}} \cdot \frac{v_{out}}{v_A}. \tag{5.180}$$

Here, v_A/v_{in} denotes the effect of voltage division between R_B and the impedance seen at the base of Q_1, and v_{out}/v_A represents the voltage gain from the base of Q_1 to the output, as already obtained in Eqs. (5.155) and (5.157). We leave the former approach for Problem 44 and continue with the latter here.

Let us first compute v_A/v_{in} with the aid of Eq. (5.162) and the model depicted in Fig. 5.39(b), as illustrated in Fig. 5.43(b). The resulting voltage divider yields

$$\frac{v_A}{v_{in}} = \frac{r_\pi + (\beta+1)R_E}{r_\pi + (\beta+1)R_E + R_B}. \tag{5.181}$$

Combining (5.155) and (5.157), we arrive at the overall gain as

$$\frac{v_{out}}{v_{in}} = \frac{r_\pi + (\beta+1)R_E}{r_\pi + (\beta+1)R_E + R_B} \cdot \frac{-g_m R_C}{1 + \left(\dfrac{1}{r_\pi} + g_m\right) R_E} \tag{5.182}$$

$$= \frac{r_\pi + (\beta+1)R_E}{r_\pi + (\beta+1)R_E + R_B} \cdot \frac{-g_m r_\pi R_C}{r_\pi + (1+\beta)R_E} \tag{5.183}$$

$$= \frac{-\beta R_C}{r_\pi + (\beta+1)R_E + R_B}. \tag{5.184}$$

To obtain a more intuitive expression, we divide the numerator and the denominator by β:

$$A_v \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_B}{\beta+1}}. \tag{5.185}$$

Compared to (5.157), this result contains only one additional term in the denominator equal to the base resistance divided by $\beta + 1$.

The above results reveal that resistances in series with the emitter and the base have similar effects on the voltage gain, but R_B is scaled down by $\beta + 1$. The significance of this observation becomes clear later.

For the stage of Fig. 5.43(a), we can define two different input impedances, one seen at the base of Q_1 and another at the left terminal of R_B (Fig. 5.44). The former is equal to

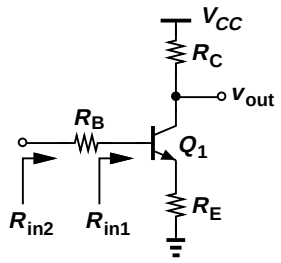


Figure 5.44 Input impedances seen at different nodes.

$$R_{in1} = r_\pi + (\beta + 1)R_E \tag{5.186}$$

and the latter,

$$R_{in2} = R_B + r_\pi + (\beta + 1)R_E. \tag{5.187}$$

In practice, R_{in1} proves more relevant and useful. We also note that the output impedance of the circuit remains equal to

$$R_{out} = R_C \tag{5.188}$$

even with $R_B \neq 0$. This is studied in Problem 45.

Example 5.26

A microphone having an output resistance of 1 kΩ generates a peak signal level of 2 mV. Design a CE stage with a bias current of 1 mA that amplifies this signal to 40 mV. Assume $R_E = 4/g_m$ and $\beta = 100$.

Solution

The following quantities are obtained: $R_B = 1\ \text{k}\Omega$, $g_m = (26\ \Omega)^{-1}$, $|A_v| = 20$, and $R_E = 104\ \Omega$. From Eq. (5.185),

$$R_C = |A_v| \left(\frac{1}{g_m} + R_E + \frac{R_B}{\beta+1} \right) \tag{5.189}$$

$$\approx 2.8\ \text{k}\Omega. \tag{5.190}$$

Exercise

Repeat the above example if the microphone output resistance is doubled.

Example 5.27

Determine the voltage gain and I/O impedances of the circuit shown in Fig. 5.45(a). Assume a very large value for C_1 and neglect the Early effect.

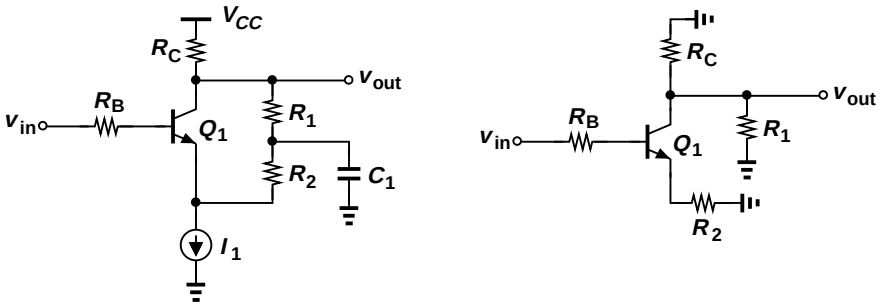


Figure 5.45 (a) CE stage example, (b) simplified circuit.

Solution

Replacing C_1 with a short circuit, I_1 with an open circuit, and V_{CC} with ac ground, we arrive at the simplified model in Fig. 5.45(b), where R_1 and R_C appear in parallel and R_2 acts as an emitter degeneration resistor. Equations (5.185)-(5.188) are therefore written respectively as

$$A_v = \frac{-(R_C||R_1)}{\dfrac{1}{g_m} + R_2 + \dfrac{R_B}{\beta+1}} \tag{5.191}$$

$$R_{in} = R_B + r_\pi + (\beta+1)R_2 \tag{5.192}$$

$$R_{out} = R_C||R_1. \tag{5.193}$$

Exercise

What happens if a very large capacitor is tied from the emitter of Q_1 to ground?

Effect of Transistor Output Resistance The analysis of the degenerated CE stage has thus far neglected the Early effect. Somewhat beyond the scope of this book, the derivation of the circuit properties in the presence of this effect is outlined in Problem 48 for the interested reader. We nonetheless explore one aspect of the circuit, namely, the output resistance, as it provides the foundation for many other topologies studied later.

Our objective is to determine the output impedance seen looking into the collector of a degenerated transistor [Fig. 5.46(a)]. Recall from Fig. 5.7 that $R_{out} = r_O$ if $R_E = 0$. Also, $R_{out} = \infty$ if $V_A = \infty$ (why?). To include the Early effect, we draw the small-signal equivalent circuit as in Fig. 5.46(b), grounding the input terminal. A common mistake here is to write $R_{out} = r_O + R_E$. Since $g_m v_\pi$ flows from the output node into P, resistors r_O and R_E are not in series. We readily note that R_E and r_π appear in parallel, and the current flowing through $R_E||r_\pi$ is equal to i_X. Thus,

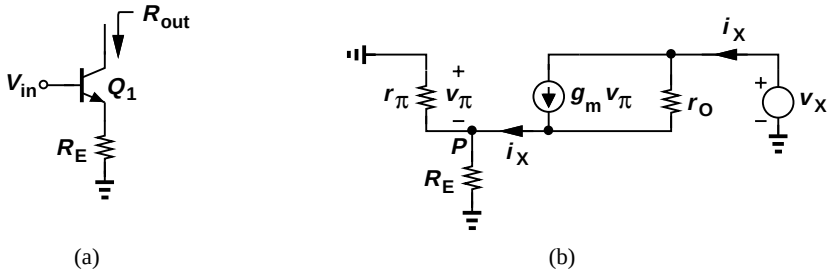


Figure 5.46 (a) Output impedance of degenerated stage, (b) equivalent circuit.

$$v_\pi = -i_X(R_E||r_\pi), \tag{5.194}$$

where the negative sign arises because the positive side of v_π is at ground. We also recognize that r_O carries a current of $i_X - g_m v_\pi$ and hence sustains a voltage of $(i_X - g_m v_\pi)r_O$. Adding this voltage to that across R_E $(= -v_\pi)$ and equating the result to v_X, we obtain

$$v_X = (i_X - g_m v_\pi)r_O - v_\pi \tag{5.195}$$

$$= [i_X + g_m i_X(R_E||r_\pi)]r_O + i_X(R_E||r_\pi). \tag{5.196}$$

It follows that

$$R_{out} = [1 + g_m(R_E||r_\pi)]r_O + R_E||r_\pi \tag{5.197}$$

$$= r_O + (g_m r_O + 1)(R_E||r_\pi). \tag{5.198}$$

Recall from (5.146) that the intrinsic gain of the transistor, $g_m r_O \gg 1$, and hence

$$R_{out} \approx r_O + g_m r_O(R_E||r_\pi) \tag{5.199}$$

$$\approx r_O[1 + g_m(R_E||r_\pi)]. \tag{5.200}$$

Interestingly, emitter degeneration *raises* the output impedance from r_O to the above value, i.e., by a factor of $1 + g_m(R_E||r_\pi)$.

The reader may wonder if the increase in the output resistance is desirable or undesirable. The "boosting" of output resistance as a result of degeneration proves extremely useful in circuit design, conferring amplifiers with a higher gain as well as creating more ideal current sources. These concepts are studied in Chapter 9.

It is instructive to examine (5.200) for two special cases $R_E \gg r_\pi$ and $R_E \ll r_\pi$. For $R_E \gg r_\pi$, we have $R_E||r_\pi \to r_\pi$ and

$$R_{out} \approx r_O(1 + g_m r_\pi) \tag{5.201}$$

$$\approx \beta r_O, \tag{5.202}$$

because $\beta \gg 1$. Thus, the maximum resistance seen at the collector of a bipolar transistor is equal to βr_O—if the degeneration impedance becomes much larger than r_π.

For $R_E \ll r_\pi$, we have $R_E || r_\pi \rightarrow R_E$ and

$$R_{out} \approx (1 + g_m R_E) r_O. \tag{5.203}$$

Thus, the output resistance is boosted by a factor of $1 + g_m R_E$.

In the analysis of circuits, we sometimes draw the transistor output resistance explicitly to emphasize its significance (Fig. 5.47). This representation, of course, assumes Q_1 itself does not contain another r_O.

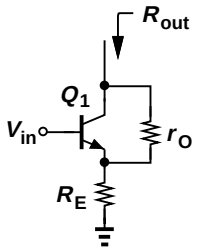


Figure 5.47 Stage with explicit depiction of r_O.

Example 5.28

We wish to design a current source having a value of 1 mA and an output resistance of 20 kΩ. The available bipolar transistor exhibits $\beta = 100$ and $V_A = 10$ V. Determine the minimum required value of emitter degeneration resistance.

Solution

Since $r_O = V_A / I_C = 10$ kΩ, degeneration must raise the output resistance by a factor of two. We postulate that the condition $R_E \ll r_\pi$ holds and write

$$1 + g_m R_E = 2. \tag{5.204}$$

That is,

$$R_E = \frac{1}{g_m} \tag{5.205}$$

$$= 26\ \Omega. \tag{5.206}$$

Note that indeed $r_\pi = \beta / g_m \gg R_E$.

Exercise

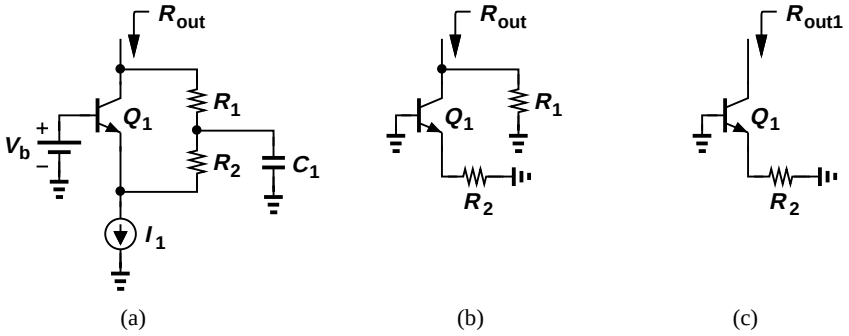
What is the output impedance if R_E is doubled?

Example 5.29

Calculate the output resistance of the circuit shown in Fig. 5.48(a) if C_1 is very large.

Solution

Replacing V_b and C_1 with an ac ground and I_1 with an open circuit, we arrive at the simplified



(a) (b) (c)

Figure 5.48 (a) CE stage example, (b) simplified circuit, (c) resistance seen at the collector.

model in Fig. 5.48(b). Since R_1 appears in parallel with the resistance seen looking into the collector of Q_1, we ignore R_1 for the moment, reducing the circuit to that in Fig. 5.48(c). In analogy with Fig. 5.40, we rewrite Eq. (5.200) as

$$R_{out1} = [1 + g_m(R_2||r_\pi)]r_O. \tag{5.207}$$

Returning to Fig. 5.48(b), we have

$$R_{out} = R_{out1}||R_1 \tag{5.208}$$

$$= \{[1 + g_m(R_2||r_\pi)]r_O\}\,||R_1. \tag{5.209}$$

Exercise

What is the output resistance if a very large capacitor is tied between the emitter of Q_1 and ground?

The procedure of progressively simplifying a circuit until it resembles a known topology proves extremely critical in our work. Called "analysis by inspection," this method obviates the need for complex small-signal models and lengthy calculations. The reader is encouraged to attempt the above example using the small-signal model of the overall circuit to appreciate the efficiency and insight provided by our intuitive approach.

Example 5.30

Determine the output resistance of the stage shown in Fig. 5.49(a).

Solution

Recall from Fig. 5.7 that the impedance seen at the collector is equal to r_O if the base and emitter are (ac) grounded. Thus, Q_2 can be replaced with r_{O2} [Fig. 5.49(b)]. From another perspective, Q_2 is reduced to r_{O2} because its base-emitter voltage is fixed by V_{b1}, yielding a zero $g_{m2}v_{\pi 2}$.

Now, r_{O2} plays the role of emitter degeneration resistance for Q_1. In analogy with Fig. 5.40(a), we rewrite Eq. (5.200) as

$$R_{out} = [1 + g_{m1}(r_{O2}||r_{\pi 1})]r_{O1}. \tag{5.210}$$

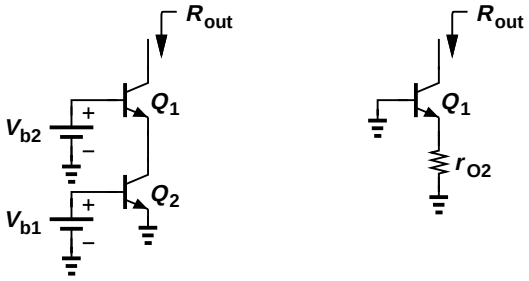


Figure 5.49 (a) CE stage example, (b) simplified circuit.

Called a "cascode" circuit, this topology is studied and utilized extensively in Chapter 9.

Exercise

Repeat the above example for a "stack" of three transistors.

CE Stage with Biasing Having learned the small-signal properties of the common-emitter amplifier and its variants, we now study a more general case wherein the circuit contains a bias network as well. We begin with simple biasing schemes described in Section 5.2 and progressively add complexity (and more robust performance) to the circuit. Let us begin with an example.

Example 5.31

A student familiar with the CE stage and basic biasing constructs the circuit shown in Fig. 5.50 to amplify the signal produced by a microphone. Unfortunately, Q_1 carries no current, failing to amplify. Explain the cause of this problem.

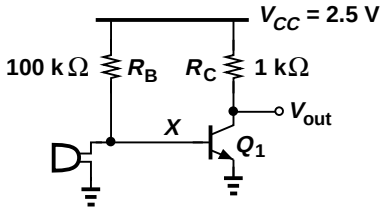


Figure 5.50 Microphone amplifier.

Solution

Many microphones exhibit a small low-frequency resistance (e.g., $< 100\ \Omega$). If used in this circuit, such a microphone creates a low resistance from the base of Q_1 to ground, forming a voltage divider with R_B and providing a very low base voltage. For example, a microphone resistance of 100 Ω yields

$$V_X = \frac{100\ \Omega}{100\ \text{k}\Omega + 100\ \Omega} \times 2.5\ \text{V} \tag{5.211}$$

$$\approx 2.5\ \text{mV}. \tag{5.212}$$

Thus, the microphone low-frequency resistance disrupts the bias of the amplifier.

Exercise

Does the circuit operate better if R_B is halved?

How should the circuit of Fig. 5.50 be fixed? Since only the *signal* generated by the microphone is of interest, a series capacitor can be inserted as depicted in Fig. 5.51 so as to isolate the dc biasing of the amplifier from the microphone. That is, the bias point of Q_1 remains independent of the resistance of the microphone because C_1 carries no bias current. The value of C_1 is chosen so that it provides a relatively low impedance (almost a short circuit) for the frequencies of interest. We say C_1 is a "coupling" capacitor and the input of this stage is "ac-coupled" or "capacitively-coupled." Many circuits employ capacitors to isolate the bias conditions from "undesirable" effects. More examples clarify this point later.

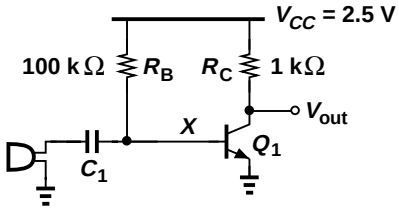


Figure 5.51 Capacitive coupling at the input of microphone amplifier.

The foregoing observation suggests that the methodology illustrated in Fig. 5.9 must include an additional rule: replace all capacitors with an open circuit for dc analysis and a short circuit for small-signal analysis.

Let us begin with the stage depicted in Fig. 5.52(a). For bias calculations, the signal source is set to zero and C_1 is opened, leading to Fig. 5.52(b). From Section 5.2.1, we have

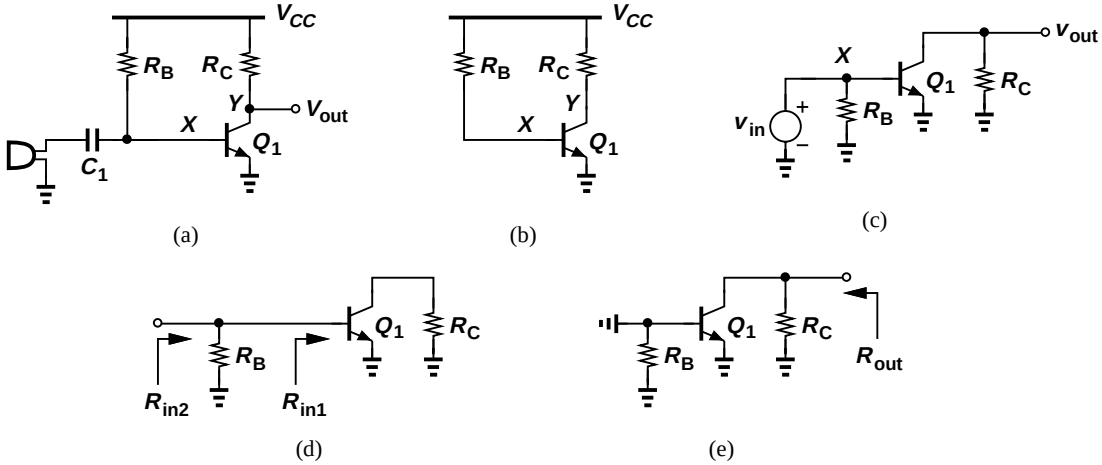


Figure 5.52 (a) Capacitive coupling at the input of a CE stage, (b) simplified stage for bias calculation, (c) simplified stage for small-signal calculation, (d) simplified circuit for input impedance calculation, (e) simplified circuit for output impedance calculation.

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B}, \tag{5.213}$$

$$V_Y = V_{CC} - \beta R_C \frac{V_{CC} - V_{BE}}{R_B}. \tag{5.214}$$

To avoid saturation, $V_Y \geq V_{BE}$.

With the bias current known, the small-signal parameters g_m, r_π, and r_O can be calculated. We now turn our attention to small-signal analysis, considering the simplified circuit of Fig. 5.52(c). Here, C_1 is replaced with a short and V_{CC} with ac ground, but Q_1 is maintained as a symbol. We attempt to solve the circuit by inspection: if unsuccessful, we will resort to using a small-signal model for Q_1 and writing KVLs and KCLs.

The circuit of Fig. 5.52(c) resembles the CE core illustrated in Fig. 5.29, except for R_B. Interestingly, R_B has no effect on the voltage at node X so long as v_{in} remains an ideal voltage source; i.e., $v_X = v_{in}$ regardless of the value of R_B. Since the voltage gain from the base to the collector is given by $v_{out}/v_X = -g_m R_C$, we have

$$\frac{v_{out}}{v_{in}} = -g_m R_C. \tag{5.215}$$

If $V_A < \infty$, then

$$\frac{v_{out}}{v_{in}} = -g_m (R_C || r_O). \tag{5.216}$$

However, the input impedance is affected by R_B [Fig. 5.52(d)]. Recall from Fig. 5.7 that the impedance seen looking into the base, R_{in1}, is equal to r_π if the emitter is grounded. Here, R_B simply appears in parallel with R_{in1}, yielding

$$R_{in2} = r_\pi || R_B. \tag{5.217}$$

Thus, the bias resistor lowers the input impedance. Nevertheless, as shown in Problem 51, this effect is usually negligible.

To determine the output impedance, we set the input source to zero [Fig. 5.52(e)]. Comparing this circuit with that in Fig. 5.32(b), we recognize that R_{out} remains unchanged:

$$R_{out} = R_C || r_O. \tag{5.218}$$

because both terminals of R_B are shorted to ground.

In summary, the bias resistor, R_B, negligibly impacts the performance of the stage shown in Fig. 5.52(a).

Example 5.32

Having learned about ac coupling, the student in Example 5.31 modifies the design to that shown in Fig. 5.53 and attempts to drive a speaker. Unfortunately, the circuit still fails. Explain why.

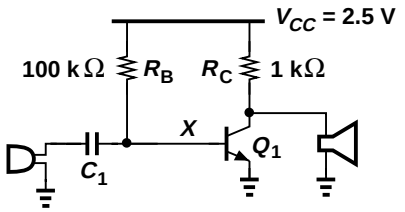


Figure 5.53 Amplifier with direct connection of speaker.

Solution

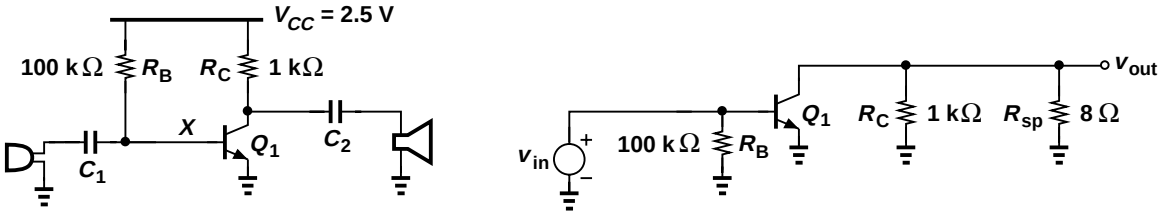
Typical speakers incorporate a solenoid (inductor) to actuate a membrane. The solenoid exhibits a very low dc resistance, e.g., less than 1 Ω. Thus, the speaker in Fig. 5.53 shorts the collector to ground, driving Q_1 into deep saturation.

Exercise

Does the circuit operate better if the speaker is tied between the output node and V_{CC}?

Example 5.33

The student applies ac coupling to the output as well [Fig. 5.54(a)] and measures the quiescent points to ensure proper biasing. The collector bias voltage is 1.5 V, indicating that Q_1 operates in the active region. However, the student still observes no gain in the circuit. (a) If $I_S = 5 \times 10^{-17}$ A and $V_A = \infty$, compute the β of the transistor. (b) Explain why the circuit provides no gain.



(a) (b)

Figure 5.54 (a) Amplifier with capacitive coupling at the input and output, (b) simplified small-signal model.

Solution

(a) A collector voltage of 1.5 V translates to a voltage drop of 1 V across R_C and hence a collector current of 1 mA. Thus,

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \tag{5.219}$$

$$= 796\,\text{mV}. \tag{5.220}$$

It follows that

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{5.221}$$

$$= 17\,\mu\text{A}, \tag{5.222}$$

and $\beta = I_C/I_B = 58.8$.

(b) Speakers typically exhibit a low impedance in the audio frequency range, e.g., 8 Ω. Drawing the ac equivalent as in Fig. 5.54(b), we note that the total resistance seen at the collector node is equal to $1\ \text{k}\Omega||8\ \Omega$, yielding a gain of

$$|A_v| = g_m(R_C||R_S) = 0.31 \tag{5.223}$$

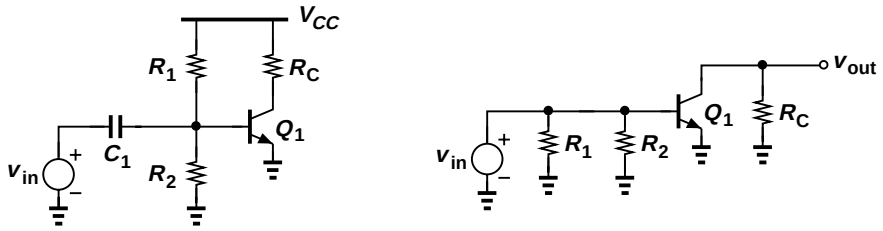
Exercise

Repeat the above example for $R_C = 500\,\Omega$.

The design in Fig. 5.54(a) exemplifies an improper interface between an amplifier and a load: the output impedance is so much higher than the load impedance that the connection of the load to the amplifier drops the gain drastically.

How can we remedy the problem of loading here? Since the voltage gain is proportional to g_m, we can bias Q_1 at a much higher current to raise the gain. This is studied in Problem 53. Alternatively, we can interpose a "buffer" stage between the CE amplifier and the speaker (Section 5.3.3).

Let us now consider the biasing scheme shown in Fig. 5.15 and repeated in Fig. 5.55(a). To determine the bias conditions, we set the signal source to zero and open the capacitor(s). Equations (5.38)-(5.41) can then be used. For small-signal analysis, the simplified circuit in Fig. 5.55(b) reveals a resemblance to that in Fig. 5.52(b), except that both R_1 and R_2 appear in parallel with the input. Thus, the voltage gain is still equal to $-g_m(R_C||r_O)$ and the input impedance is given by



(a) (b)

Figure 5.55 (a) Biased stage with capacitive coupling, (b) simplified circuit.

$$R_{in} = r_\pi||R_1||R_2. \tag{5.224}$$

The output resistance is equal to $R_C||r_O$.

We next study the more robust biasing scheme of Fig. 5.19, repeated in Fig. 5.56(a) along with an input coupling capacitor. The bias point is determined by opening C_1 and following Eqs. (5.52) and (5.53). With the collector current known, the small-signal parameters of Q_1 can be computed. We also construct the simplified ac circuit shown in Fig. 5.56(b), noting that the voltage gain is not affected by R_1 and R_2 and remains equal to

$$A_v = \frac{-R_C}{\dfrac{1}{g_m} + R_E}, \tag{5.225}$$

where Early effect is neglected. On the other hand, the input impedance is lowered to:

$$R_{in} = [r_\pi + (\beta+1)R_E]||R_1||R_2, \tag{5.226}$$

whereas the output impedance remains equal to R_C if $V_A = \infty$.

As explained in Section 5.2.3, the use of emitter degeneration can effectively stabilize the bias point despite variations in β and I_S. However, as evident from (5.225), degeneration also lowers

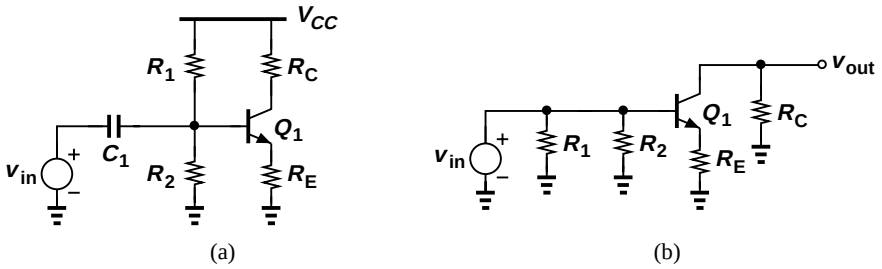


Figure 5.56 (a) Degenerated stage with capacitive coupling, (b) simplified circuit.

the gain. Is it possible to apply degeneration to biasing but *not* to the signal? Illustrated in Fig. 5.57 is such a topology, where C_2 is large enough to act as a short circuit for signal frequencies of interest. We can therefore write

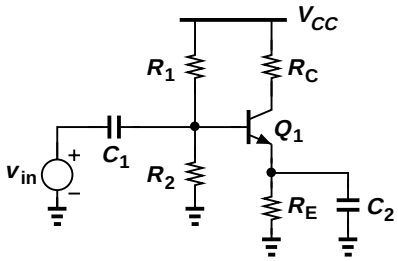


Figure 5.57 Use of capacitor to eliminate degeneration.

$$A_v = -g_m R_C \tag{5.227}$$

and

$$R_{in} = r_\pi || R_1 || R_2 \tag{5.228}$$

$$R_{out} = R_C. \tag{5.229}$$

Example 5.34

Design the stage of Fig. 5.57 to satisfy the following conditions: $I_C = 1$ mA, voltage drop across $R_E = 400$ mV, voltage gain $= 20$ in the audio frequency range (20 Hz to 20 kHz), input impedance > 2 kΩ. Assume $\beta = 100$, $I_S = 5 \times 10^{-16}$, and $V_{CC} = 2.5$ V.

Solution

With $I_C = 1$ mA $\approx I_E$, the value of R_E is equal to 400 Ω. For the voltage gain to remain unaffected by degeneration, the maximum impedance of C_1 must be much smaller than $1/g_m = 26\ \Omega$.[8] Occurring at 20 Hz, the maximum impedance must remain below roughly $0.1 \times (1/g_m) = 2.6\ \Omega$:

$$\frac{1}{C_2 \omega} \leq \frac{1}{10} \cdot \frac{1}{g_m} \text{ for } \omega = 2\pi \times 20 \text{ Hz}. \tag{5.230}$$

[8] A common mistake here is to make the impedance of C_1 much less than R_E.

Thus,

$$C_2 \geq 6120\,\mu\text{F}. \tag{5.231}$$

(This value is unrealistically large, requiring modification of the design.) We also have

$$|A_v| = g_m R_C = 20, \tag{5.232}$$

obtaining

$$R_C = 512\,\Omega. \tag{5.233}$$

Since the voltage across R_E is equal to 400 mV and $V_{BE} = V_T \ln(I_C/I_S) = 736$ mV, we have $V_X = 1.14$ V. Also, with a base current of 10 μA, the current flowing through R_1 and R_2 must exceed 100 μA to lower sensitivity to β:

$$\frac{V_{CC}}{R_1 + R_2} > 10 I_B \tag{5.234}$$

and hence

$$R_1 + R_2 < 25\ \text{k}\Omega. \tag{5.235}$$

Under this condition,

$$V_X \approx \frac{R_2}{R_1 + R_2} V_{CC} = 1.14\ \text{V}, \tag{5.236}$$

yielding

$$R_2 = 11.4\ \text{k}\Omega \tag{5.237}$$

$$R_1 = 13.6\ \text{k}\Omega. \tag{5.238}$$

We must now check to verify that this choice of R_1 and R_2 satisfies the condition $R_{in} > 2\ \text{k}\Omega$. That is,

$$R_{in} = r_\pi || R_1 || R_2 \tag{5.239}$$

$$= 1.85\ \text{k}\Omega. \tag{5.240}$$

Unfortunately, R_1 and R_2 lower the input impedance excessively. To remedy the problem, we can allow a smaller current through R_1 and R_2 than $10 I_B$, at the cost of creating more sensitivity to β. For example, if this current is set to $5 I_B = 50$ μA and we still neglect I_B in the calculation of V_X,

$$\frac{V_{CC}}{R_1 + R_2} > 5 I_B \tag{5.241}$$

and

$$R_1 + R_2 < 50\ \text{k}\Omega. \tag{5.242}$$

Consequently,

$$R_2 = 22.4\,\text{k}\Omega \tag{5.243}$$

$$R_1 = 27.2\,\text{k}\Omega, \tag{5.244}$$

giving

$$R_{in} = 2.14\,\text{k}\Omega. \tag{5.245}$$

Exercise

Redesign the above stage for a gain of 10 and compare the results.

We conclude our study of the CE stage with a brief look at the more general case depicted in Fig. 5.58(a), where the input signal source exhibits a finite resistance and the output is tied to a load R_L. The biasing remains identical to that of Fig. 5.56(a), but R_S and R_L lower the voltage gain v_{out}/v_{in}. The simplified ac circuit of Fig. 5.58(b) reveals V_{in} is attenuated by the voltage division between R_S and the impedance seen at node X, $R_1||R_2||[r_\pi + (\beta+1)R_E]$, i.e.,

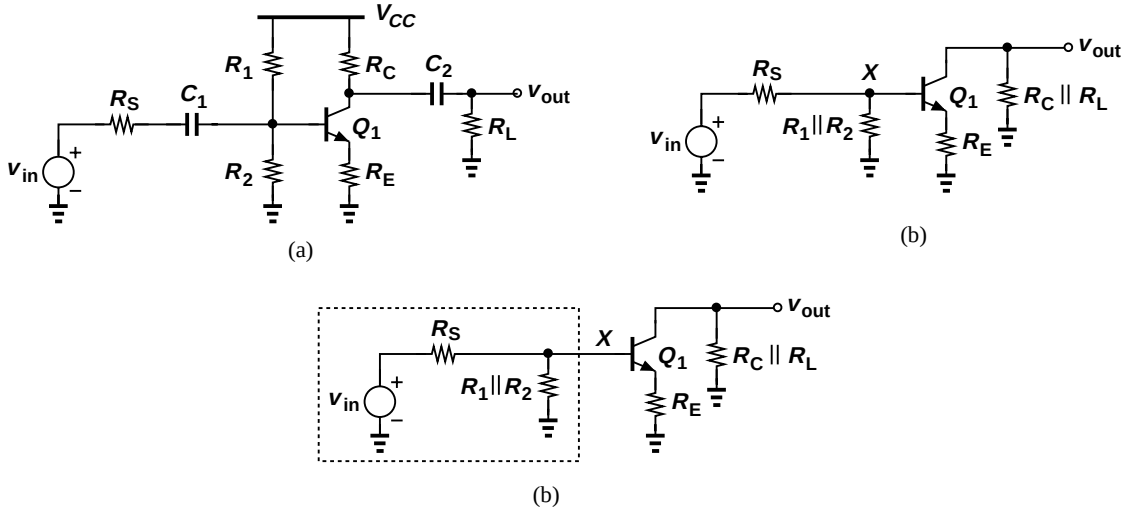


Figure 5.58 (a) General CE stage, (b) simplified circuit, (c) Thevenin model of input network.

$$\frac{v_X}{v_{in}} = \frac{R_1||R_2||[r_\pi + (\beta+1)R_E]}{R_1||R_2||[r_\pi + (\beta+1)R_E] + R_S}. \tag{5.246}$$

The voltage gain from v_{in} to the output is given by

$$\frac{v_{out}}{v_{in}} = \frac{v_X}{v_{in}} \cdot \frac{v_{out}}{v_X} \tag{5.247}$$

$$= -\frac{R_1||R_2||[r_\pi + (\beta+1)R_E]}{R_1||R_2||[r_\pi + (\beta+1)R_E] + R_S} \frac{R_C||R_L}{\dfrac{1}{g_m} + R_E}. \tag{5.248}$$

As expected, lower values of R_1 and R_2 reduce the gain.

The above computation views the input network as a voltage divider. Alternatively, we can utilize a Thevenin equivalent to include the effect of R_S, R_1, and R_2 on the voltage gain. Illustrated in Fig. 5.58(c), the idea is to replace v_{in}, R_S and $R_1||R_2$ with v_{Thev} and R_{Thev}:

$$v_{Thev} = \frac{R_1||R_2}{R_1||R_2 + R_S} v_{in} \tag{5.249}$$

$$R_{Thev} = R_S||R_1||R_2. \tag{5.250}$$

The resulting circuit resembles that in Fig. 5.43(a) and follows Eq. (5.185):

$$A_v = -\frac{R_C||R_L}{\dfrac{1}{g_m} + R_E + \dfrac{R_{Thev}}{\beta+1}} \cdot \frac{R_1||R_2}{R_1||R_2 + R_S}, \tag{5.251}$$

where the second fraction on the right accounts for the voltage attenuation given by Eq. (5.249). The reader is encouraged to prove that (5.248) and (5.251) are identical.

The two approaches described above exemplify analysis techniques used to solve circuits and gain insight. Neither requires drawing the small-signal model of the transistor because the reduced circuits can be "mapped" into known topologies.

Figure 5.59 summarizes the concepts studied in this section.

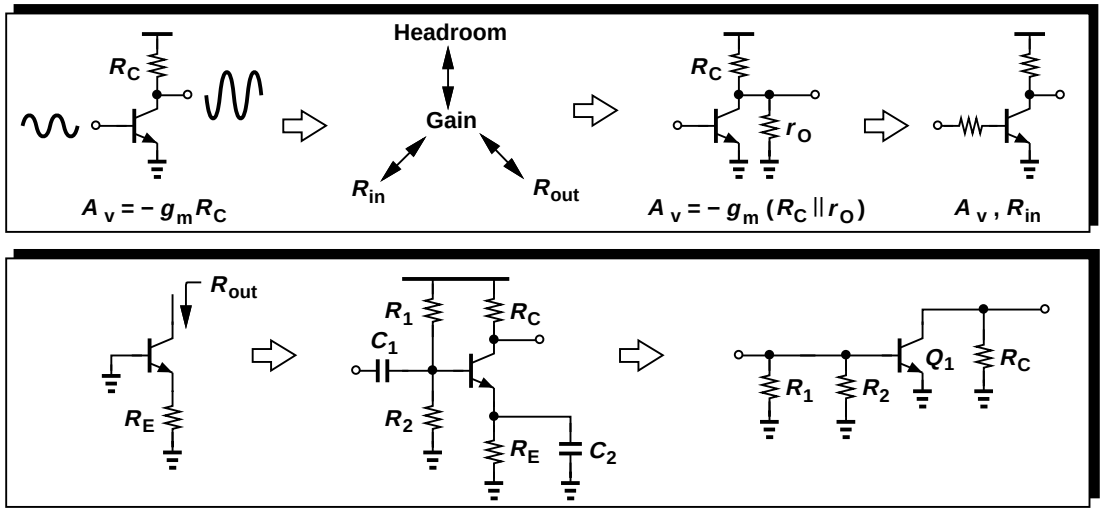


Figure 5.59 Summary of concepts studied thus far.

5.3.2 Common-Base Topology

Following our extensive study of the CE stage, we now turn our attention to the "common-base" (CB) topology. Nearly all of the concepts described for the CE configuration apply here as well. We therefore follow the same train of thought, but at a slightly faster pace.

Given the amplification capabilities of the CE stage, the reader may wonder why we study other amplifier topologies. As we will see, other configurations provide different circuit properties that are preferable to those of the CE stage in some applications. The reader is encouraged to review Examples 5.2-5.4, their resulting rules illustrated in Fig. 5.7, and the possible topologies in Fig. 5.28 before proceeding further.

Figure 5.60 shows the CB stage. The input is applied to the emitter and the output is sensed at the collector. Biased at a proper voltage, the base acts as ac ground and hence as a node "common" to the input and output ports. As with the CE stage, we first study the core and subsequently add the biasing elements.

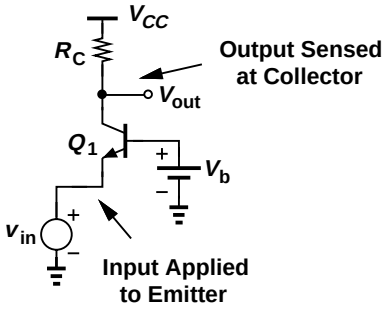


Figure 5.60 Common-base stage.

Analysis of CB Core How does the CB stage of Fig. 5.61(a) respond to an input signal?[9] If V_{in} goes up by a small amount ΔV, the base-emitter voltage of Q_1 *decreases* by the same amount because the base voltage is fixed. Consequently, the collector current falls by $g_m \Delta V$, allowing V_{out} to *rise* by $g_m \Delta V R_C$. We therefore surmise that the small-signal voltage gain is equal to

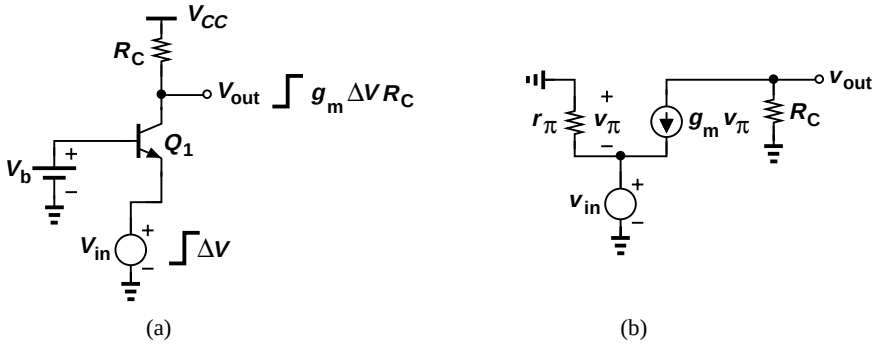


Figure 5.61 (a) Response of CB stage to small input change, (b) small-signal model.

$$A_v = g_m R_C. \tag{5.252}$$

Interestingly, this expression is identical to the gain of the CE topology. Unlike the CE stage, however, this circuit exhibits a *positive* gain because an increase in V_{in} leads to an increase in V_{out}.

Let us confirm the above results with the aid of the small-signal equivalent depicted in Fig. 5.61(b), where the Early effect is neglected. Beginning with the output node, we equate the current flowing through R_C to $g_m v_\pi$:

$$-\frac{v_{out}}{R_C} = g_m v_\pi, \tag{5.253}$$

[9] Note that the topologies of Figs. 5.60-5.61(a) are identical even though Q_1 is drawn differently.

obtaining $v_\pi = -v_{out}/(g_m R_C)$. Considering the input node next, we recognize that $v_\pi = -v_{in}$. It follows that

$$\frac{v_{out}}{v_{in}} = g_m R_C. \tag{5.254}$$

As with the CE stage, the CB topology suffers from trade-offs between the gain, the voltage headroom, and the I/O impedances. We first examine the circuit's headroom limitations. How should the base voltage, V_b, in Fig. 5.61(a) be chosen? Recall that the operation in the active region requires $V_{BE} > 0$ and $V_{BC} \leq 0$ (for npn devices). Thus, V_b must remain *higher* than the input by about 800 mV, and the output must remain higher than or equal to V_b. For example, if the dc level of the input is zero (Fig. 5.62), then the output must not fall below approximately 800 mV, i.e., the voltage drop across R_C cannot exceed $V_{CC} - V_{BE}$. Similar to the CE stage limitation, this condition translates to

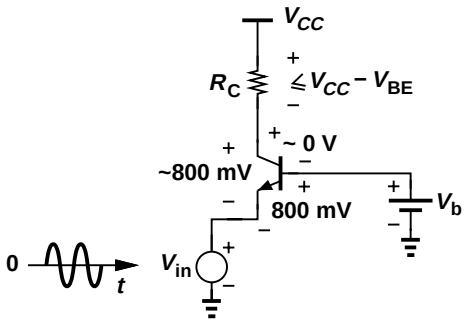


Figure 5.62 Voltage headroom in CB stage.

$$A_v = \frac{I_C}{V_T} \cdot R_C \tag{5.255}$$

$$= \frac{V_{CC} - V_{BE}}{V_T}. \tag{5.256}$$

Example 5.35

The voltage produced by an electronic thermometer is equal to 600 mV at room temperature. Design a CB stage to sense the thermometer voltage and amplify the change with maximum gain. Assume $V_{CC} = 1.8$ V, $I_C = 0.2$ mA, $I_S = 5 \times 10^{-17}$ A, and $\beta = 100$.

Solution

Illustrated in Fig. 5.63(a), the circuit must operate properly with an input level of 600 mV. Thus, $V_b = V_{BE} + 600\ \text{mV} = V_T \ln(I_C/I_S) + 600\ \text{mV} = 1.354$ V. To avoid saturation, the collector voltage must not fall below the base voltage, thereby allowing a maximum voltage drop across R_C equal to $1.8\ \text{V} - 1.354\ \text{V} = 0.446$ V. We can then write

$$A_v = g_m R_C \tag{5.257}$$

$$= \frac{I_C R_C}{V_T} \tag{5.258}$$

$$= 17.2. \tag{5.259}$$

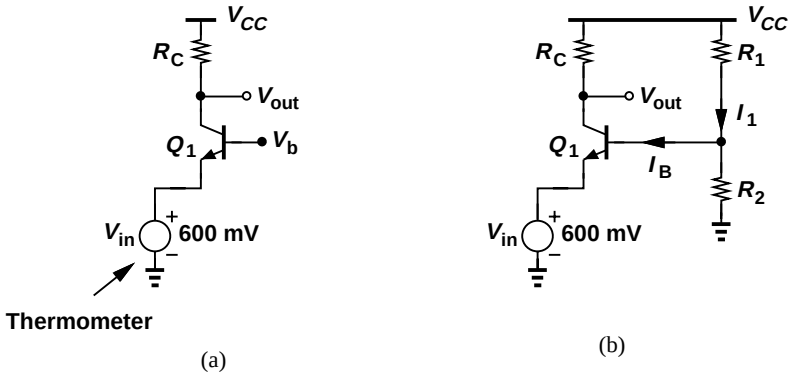


Figure 5.63 (a) CB stage sensing an input, (b) bias network for base.

The reader is encouraged to repeat the problem with $I_C = 0.4$ mA to verify that the maximum gain remains relatively independent of the bias current.[10]

We must now generate V_b. A simple approach is to employ a resistive divider as depicted in Fig. 5.63(b). To lower sensitivity to β, we choose $I_1 \approx 10I_B \approx 20\ \mu\text{A} \approx V_{CC}/(R_1 + R_2)$. Thus, $R_1 + R_2 = 90\ \text{k}\Omega$. Also,

$$V_b \approx \frac{R_2}{R_1 + R_2} V_{CC} \tag{5.260}$$

and hence

$$R_2 = 67.7\ \text{k}\Omega \tag{5.261}$$

$$R_1 = 22.3\ \text{k}\Omega. \tag{5.262}$$

Exercise

Repeat the above example if the thermometer voltage is 300 mV.

Let us now compute the I/O impedances of the CB topology so as to understand its capabilities in interfacing with preceding and following stages. The rules illustrated in Fig. 5.7 prove extremely useful here, obviating the need for small-signal equivalent circuits. Shown in Fig. 5.64(a), the simplified ac circuit reveals that R_{in} is simply the impedance seen looking into the emitter with the base at ac ground. From the rules in Fig. 5.7, we have

$$R_{in} = \frac{1}{g_m} \tag{5.263}$$

if $V_A = \infty$. The input impedance of the CB stage is therefore relatively *low*, e.g., 26 Ω for $I_C = 1$ mA (in sharp contrast to the corresponding value for a CE stage, β/g_m).

[10] This example serves only as an illustration of the CB stage. A CE stage may prove more suited to sensing a thermometer voltage.

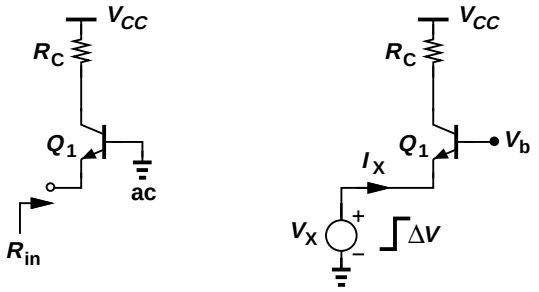


Figure 5.64 (a) Input impedance of CB stage, (b) response to a small change in input.

The input impedance of the CB stage can also be determined intuitively [Fig. 5.64(b)]. Suppose a voltage source V_X tied to the emitter of Q_1 changes by a small amount ΔV. The base-emitter voltage therefore changes by the same amount, leading to a change in the collector current equal to $g_m \Delta V$. Since the collector current flows through the input source, the current supplied by V_X also changes by $g_m \Delta V$. Consequently, $R_{in} = \Delta V_X / \Delta I_X = 1/g_m$.

Does an amplifier with a low input impedance find any practical use? Yes, indeed. For example, many stand-alone high-frequency amplifiers are designed with an input resistance of 50 Ω to provide "impedance matching" between modules in a cascade and the transmission lines (traces on a printed-circuit board) connecting the modules (Fig. 5.65).[11]

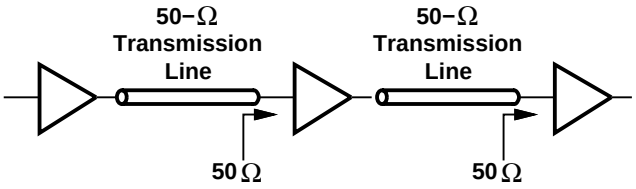


Figure 5.65 System using transmission lines.

The output impedance of the CB stage is computed with the aid of Fig. 5.66, where the input voltage source is set to zero. We note that $R_{out} = R_{out1} || R_C$, where R_{out1} is the impedance seen at the collector with the emitter grounded. From the rules of Fig. 5.7, we have $R_{out1} = r_O$ and hence

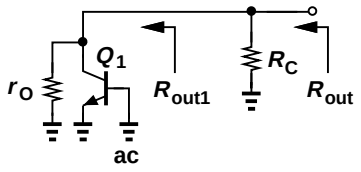


Figure 5.66 Output impedance of CB stage.

$$R_{out} = r_O || R_C \tag{5.264}$$

[11] If the input impedance of each stage is not matched to the characteristic impedance of the preceding transmission line, then "reflections" occur, corrupting the signal or at least creating dependence on the length of the lines.

or

$$R_{out} = R_C \text{ if } V_A = \infty. \tag{5.265}$$

Example 5.36

A common-base amplifier is designed for an input impedance of R_{in} and an output impedance of R_{out}. Neglecting the Early effect, determine the voltage gain of the circuit.

Solution

Since $R_{in} = 1/g_m$ and $R_{out} = R_C$, we have

$$A_v = \frac{R_{out}}{R_{in}}. \tag{5.266}$$

Exercise

Compare this value with that obtained for the CE stage.

From Eqs. (5.256) and (5.266), we conclude that the CB stage exhibits a set of trade-offs similar to those depicted in Fig. 5.33 for the CE amplifier.

It is instructive to study the behavior of the CB topology in the presence of a finite source resistance. Shown in Fig. 5.67, such a circuit suffers from signal attenuation from the input to node X, thereby providing a smaller voltage gain. More specifically, since the impedance seen looking into the emitter of Q_1 (with the base grounded) is equal to $1/g_m$ (for $V_A = \infty$), we have

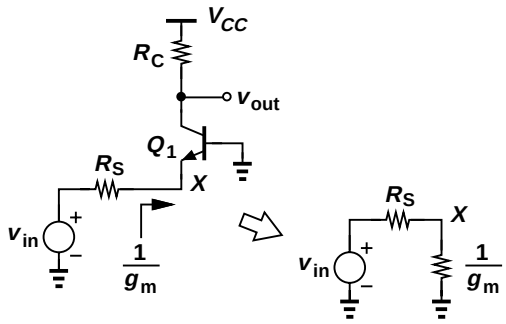


Figure 5.67 CB stage with source resistance.

$$v_X = \frac{\dfrac{1}{g_m}}{R_S + \dfrac{1}{g_m}} v_{in} \tag{5.267}$$

$$= \frac{1}{1 + g_m R_S} v_{in}. \tag{5.268}$$

We also recall from Eq. (5.254) that the gain from the emitter to the output is given by

$$\frac{v_{out}}{v_X} = g_m R_C. \tag{5.269}$$

It follows that

$$\frac{v_{out}}{v_{in}} = \frac{g_m R_C}{1 + g_m R_S} \tag{5.270}$$

$$= \frac{R_C}{\frac{1}{g_m} + R_S}, \tag{5.271}$$

a result identical to that of the CE stage (except for a negative sign) if R_S is viewed as an emitter degeneration resistor.

Example 5.37

A common-base stage is designed to amplify an RF signal received by a 50-Ω antenna. Determine the required bias current if the input impedance of the amplifier must "match" the impedance of the antenna. What is the voltage gain if the CB stage also *drives* a 50-Ω load? Assume $V_A = \infty$.

Solution

Figure 5.68 depicts the amplifier[12] and the equivalent circuit with the antenna modeled by a

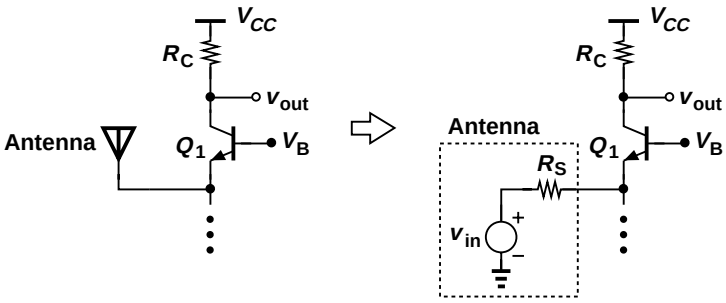


Figure 5.68 (a) CB stage sensing a signal received by an antenna, (b) equivalent circuit.

voltage source, v_{in}, and a resistance, $R_S = 50\ \Omega$. For impedance matching, it is necessary that the input impedance of the CB core, $1/g_m$, be equal to R_S, and hence

$$I_C = g_m V_T \tag{5.272}$$

$$= 0.52\ \text{mA}. \tag{5.273}$$

If R_C itself is replaced by a 50-Ω load, then Eq. (5.271) reveals that

$$A_v = \frac{R_C}{\frac{1}{g_m} + R_S} \tag{5.274}$$

$$= \frac{1}{2}. \tag{5.275}$$

The circuit is therefore not suited to driving a 50-Ω load directly.

[12] The dots denote the need for biasing circuitry, as described later in this section.

Exercise

What is the voltage gain if a 50-Ω resistor is also tied from the emitter of Q_1 to ground?

Another interesting point of contrast between the CE and CB stages relates to their current gains. The CB stage displays a current gain of *unity* because the current flowing into the emitter simply emerges from the collector (if the base current is neglected). On the other hand, as mentioned in Section 5.3.1, $A_I = \beta$ for the CE stage. In fact, in the above example, $i_{in} = v_{in}/(R_S + 1/g_m)$, which upon flowing through R_C, yields $v_{out} = R_C v_{in}/(R_S + 1/g_m)$. It is thus not surprising that the voltage gain does not exceed 0.5 if $R_C \leq R_S$.

As with the CE stage, we may desire to analyze the CB topology in the general case: with emitter degeneration, $V_A < \infty$, and a resistance in series with the base [Fig. 5.69(a)]. Outlined in Problem 64, this analysis is somewhat beyond the scope of this book. Nevertheless, it is in-

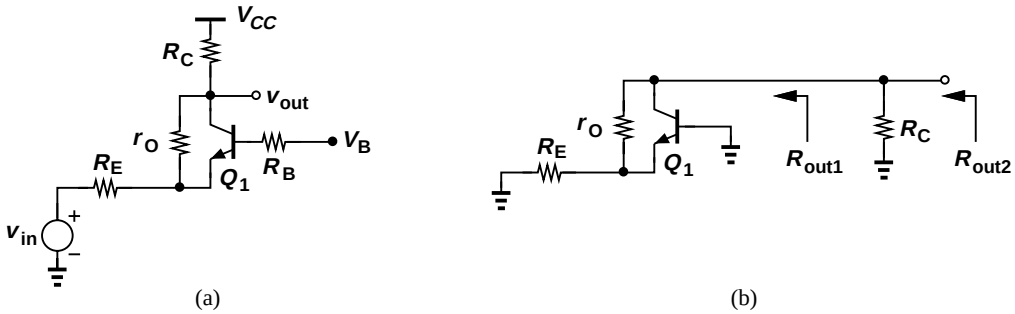


Figure 5.69 (a) General CB stage, (b) output impedance seen at different nodes.

structive to consider a special case where $R_B = 0$ but $V_A < \infty$, and we wish to compute the output impedance. As illustrated in Fig. 5.69(b), R_{out} is equal to R_C in parallel with the impedance seen looking into the collector, R_{out1}. But R_{out1} is identical to the output resistance of an emitter-degenerated *common emitter* stage, i.e., Fig. 5.46, and hence given by Eq. (5.197):

$$R_{out1} = [1 + g_m(R_E||r_\pi)]r_O + (R_E||r_\pi). \tag{5.276}$$

It follows that

$$R_{out} = R_C||\{[1 + g_m(R_E||r_\pi)]r_O + (R_E||r_\pi)\}. \tag{5.277}$$

The reader may have recognized that the output impedance of the CB stage is equal to that of the CE stage. Is this true in general? Recall that the output impedance is determined by setting the input source to zero. In other words, when calculating R_{out}, we have no knowledge of the input terminal of the circuit, as illustrated in Fig. 5.70 for CE and CB stages. It is therefore no coincidence that the output impedances are identical *if* the same assumptions are made for both circuits (e.g., identical values of V_A and emitter degeneration).

Example 5.38

Old wisdom says "the output impedance of the CB stage is substantially higher than that of the CE stage." This claim is justified by the tests illustrated in Fig. 5.71. If a constant current is injected into the base while the collector voltage is varied, I_C exhibits a slope equal to r_O^{-1} [Fig. 5.71(a)]. On the other hand, if a constant current is drawn from the emitter, I_C displays much less dependence on the collector voltage. Explain why these tests do not represent practical situations.

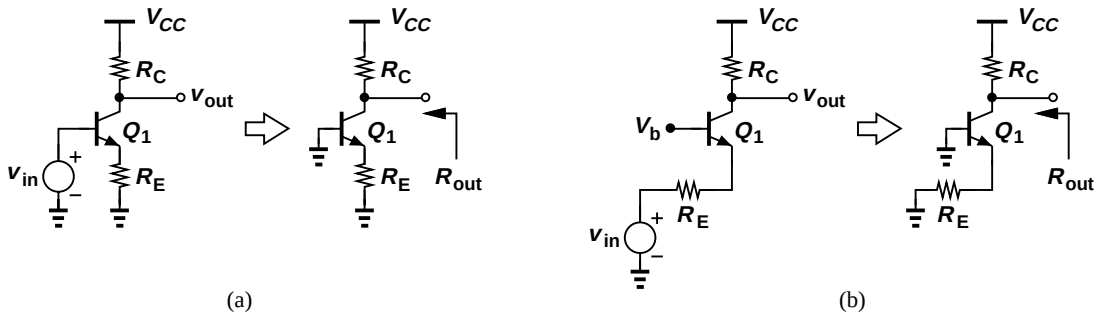


Figure 5.70 (a) CE stage and (b) CB stage simplified for output impedance calculation.

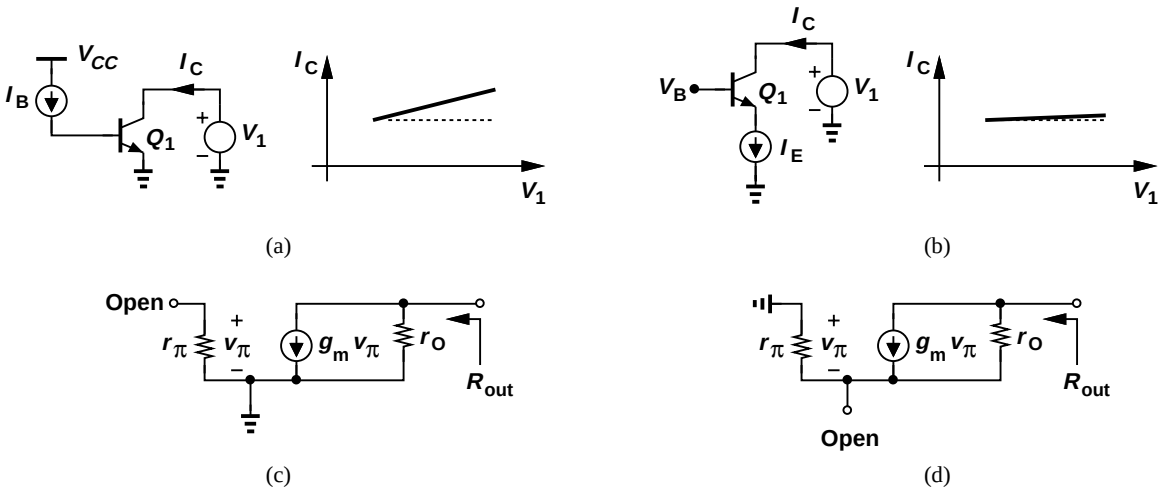


Figure 5.71 (a) Resistance seens at collector with emitter grounded, (b) resistance seen at collector with an ideal current source in emitter, (c) small-signal model of (a), (d) small-signal model of (b).

Solution

The principal issue in these tests relates to the use of *current* sources to drive each stage. From a small-signal point of view, the two circuits reduce to those depicted in Figs. 5.71(c) and (d), with current sources I_B and I_E replaced with open circuits because they are constant. In Fig. 5.71(c), the current through r_π is zero, yielding $g_m v_\pi = 0$ and hence $R_{out} = r_O$. On the other hand, Fig. 5.71(d) resembles an emitter-degenerated stage (Fig. 5.46) with an infinite emitter resistance, exhibiting an output resistance of

$$R_{out} = [1 + g_m(R_E||r_\pi)]r_O + (R_E||r_\pi) \tag{5.278}$$

$$= (1 + g_m r_\pi)r_O + r_\pi \tag{5.279}$$

$$\approx \beta r_O + r_\pi, \tag{5.280}$$

which is, of course, much greater than r_O. In practice, however, each stage may be driven by a *voltage* source having a finite impedance, making the above comparison irrelevant.

Exercise

Repeat the above example if a resistor of value R_1 is inserted in series with the emitter.

Another special case of the topology shown in Fig. 5.69(a) occurs if $V_A = \infty$ but $R_B > 0$. Since this case does not reduce to any of the configurations studied earlier, we employ the small-signal model shown in Fig. 5.72 to study its behavior. As usual, we write $g_m v_\pi = -v_{out}/R_C$ and hence $v_\pi = -v_{out}/(g_m R_C)$. The current flowing through r_π (and R_B) is then equal to $v_\pi/r_\pi = -v_{out}/(g_m r_\pi R_C) = -v_{out}/(\beta R_C)$. Multiplying this current by $R_B + r_\pi$, we obtain the voltage at node P:

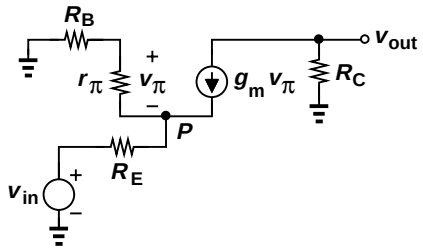


Figure 5.72 CB stage with base resistance.

$$v_P = -\frac{-v_{out}}{\beta R_C}(R_B + r_\pi) \tag{5.281}$$

$$= \frac{v_{out}}{\beta R_C}(R_B + r_\pi). \tag{5.282}$$

We also write a KCL at P:

$$\frac{v_\pi}{r_\pi} + g_m v_\pi = \frac{v_P - v_{in}}{R_E}; \tag{5.283}$$

that is,

$$\left(\frac{1}{r_\pi} + g_m\right)\frac{-v_{out}}{g_m R_C} = \frac{\dfrac{v_{out}}{\beta R_C}(R_B + r_\pi) - v_{in}}{R_E}. \tag{5.284}$$

It follows that

$$\frac{v_{out}}{v_{in}} = \frac{\beta R_C}{(\beta+1)R_E + R_B + r_\pi}. \tag{5.285}$$

Dividing the numerator and denominator by $\beta + 1$, we have

$$\frac{v_{out}}{v_{in}} \approx \frac{R_C}{R_E + \dfrac{R_B}{\beta+1} + \dfrac{1}{g_m}}. \tag{5.286}$$

As expected, the gain is positive. Furthermore, this expression is identical to that in (5.185) for the CE stage. Figure 5.73 illustrates the results, revealing that, except for a negative sign, the two stages exhibit equal gains. Note that R_B degrades the gain and is not added to the circuit deliberately. As explained later in this section, R_B may arise from the biasing network.

Let us now determine the input impedance of the CB stage in the presence of a resistance in series with the base, still assuming $V_A = \infty$. From the small-signal equivalent circuit shown in

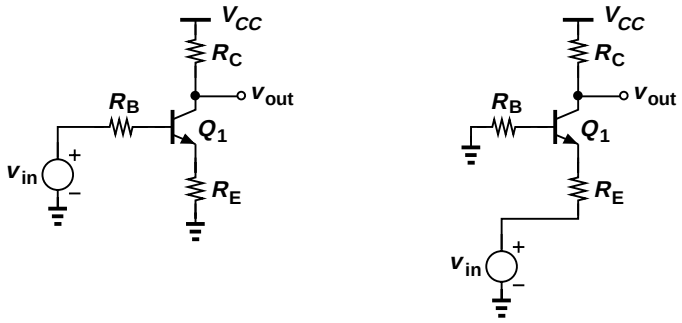


Figure 5.73 Comparison of CE and CB stages with base resistance.

Fig. 5.74, we recognize that r_π and R_B form a voltage divider, thereby producing[13]

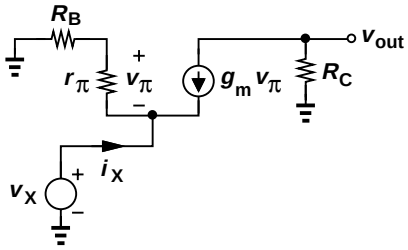


Figure 5.74 Input impedance of CB stage with base resistance.

$$v_\pi = -\frac{r_\pi}{r_\pi + R_B} v_X. \tag{5.287}$$

Moreover, KCL at the input node gives

$$\frac{v_\pi}{r_\pi} + g_m v_\pi = -i_X. \tag{5.288}$$

Thus,

$$\left(\frac{1}{r_\pi} + g_m\right) \frac{-r_\pi}{r_\pi + R_B} v_X = -i_X \tag{5.289}$$

and

$$\frac{v_X}{i_X} = \frac{r_\pi + R_B}{\beta + 1} \tag{5.290}$$

$$\approx \frac{1}{g_m} + \frac{R_B}{\beta + 1}. \tag{5.291}$$

Note that $R_{in} = 1/g_m$ if $R_B = 0$, an expected result from the rules illustrated in Fig. 5.7. Interestingly, the base resistance is divided by $\beta + 1$ when "seen" from the emitter. This is in contrast to the case of emitter degeneration, where the emitter resistance is *multiplied* by $\beta + 1$

[13] Alternatively, the current through $r_\pi + R_B$ is equal to $v_X/(r_\pi + R_B)$, yielding a voltage of $-r_\pi v_X/(r_\pi + R_B)$ across r_π.

when seen from the base. Figure 5.75 summarizes the two cases. Interestingly, these results remain independent of R_C if $V_A = \infty$.

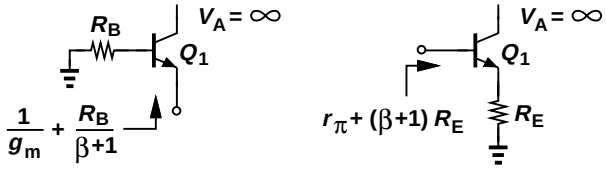


Figure 5.75 Impedance seen at the emitter or base of a transistor.

Example 5.39

Determine the impedance seen at the emitter of Q_2 in Fig. 5.76(a) if the two transistors are identical and $V_A = \infty$.

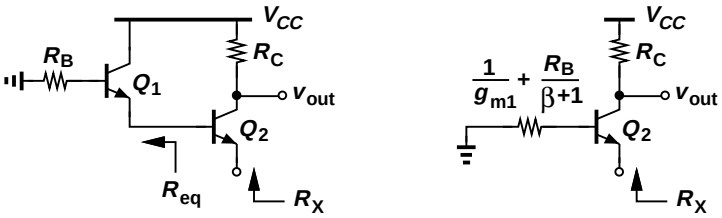


Figure 5.76 (a) Example of CB stage, (b) simplified circuit.

Solution

The circuit employs Q_2 as a common-base device, but with its base tied to a finite series resistance equal to that seen at the emitter of Q_1. Thus, we must first obtain the equivalent resistance R_{eq}, which from Eq. (5.291) is simply equal to

$$R_{eq} = \frac{1}{g_{m1}} + \frac{R_B}{\beta + 1}. \tag{5.292}$$

Reducing the circuit to that shown in Fig. 5.76(b), we have

$$R_X = \frac{1}{g_{m2}} + \frac{R_{eq}}{\beta + 1} \tag{5.293}$$

$$= \frac{1}{g_{m2}} + \frac{1}{\beta + 1}\left(\frac{1}{g_{m1}} + \frac{R_B}{\beta + 1}\right). \tag{5.294}$$

Exercise

What happens if a resistor of value R_1 is placed in series with the collector of Q_1?

CB Stage with Biasing Having learned the small-signal properties of the CB core, we now extend our analysis to the circuit including biasing. An example proves instructive at this point.

Example 5.40

The student in Example 5.31 decides to incorporate ac coupling at the input of a CB stage to ensure the bias is not affected by the signal source, drawing the design as shown in Fig. 5.77. Explain why this circuit does not work.

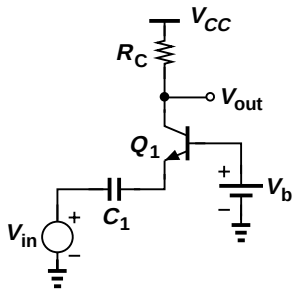


Figure 5.77 CB stage lacking bias current.

Solution

Unfortunately, the design provides no dc path for the emitter current of Q_1, forcing a zero bias current and hence a zero transconductance. The situation is similar to the CE counterpart in Example 5.5, where no base current can be supported.

Exercise

In what region does Q_1 operate if $V_b = V_{CC}$?

Example 5.41

Somewhat embarrassed, the student quickly connects the emitter to ground so that $V_{BE} = V_b$ and a reasonable collector current can be established (Fig. 5.78). Explain why "haste makes waste."

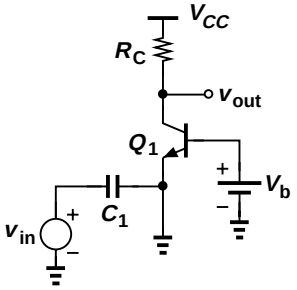


Figure 5.78 CB stage with emitter shorted to ground.

Solution

As with Example 5.6, the student has shorted the *signal* to ac ground. That is, the emitter voltage is equal to zero regardless of the value of v_{in}, yielding $v_{out} = 0$.

Exercise

Does the circuit operate better if V_b is raised?

The above examples imply that the emitter can remain neither open nor shorted to ground, thereby requiring some bias element. Shown in Fig. 5.79(a) is an example, where R_E provides a path for the bias current at the cost of lowering the input impedance. We recognize that R_{in} now consists of two *parallel* components: (1) $1/g_m$, seen looking "up" into the emitter (with the base at ac ground) and (2) R_E, seen looking "down." Thus,

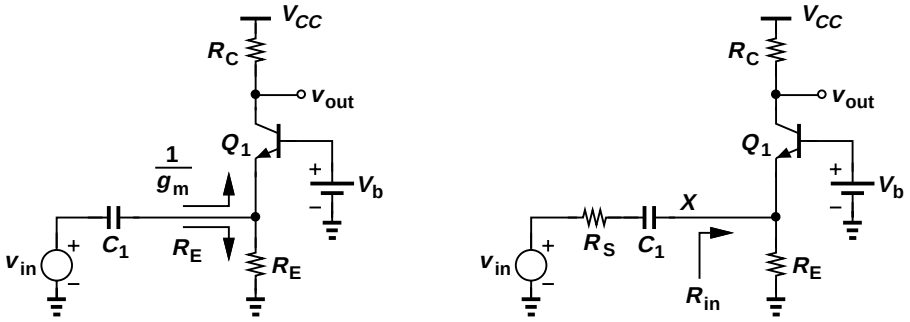


Figure 5.79 (a) CB stage with biasing, (b) inclusion of source resistance.

$$R_{in} = \frac{1}{g_m} || R_E. \tag{5.295}$$

As with the input biasing network in the CE stage (Fig. 5.58), the reduction in R_{in} manifests itself if the source voltage exhibits a finite output resistance. Depicted in Fig. 5.79(b), such a circuit attenuates the signal, lowering the overall voltage gain. Following the analysis illustrated in Fig. 5.67, we can write

$$\frac{v_X}{v_{in}} = \frac{R_{in}}{R_{in} + R_S} \tag{5.296}$$

$$= \frac{\frac{1}{g_m} || R_E}{\frac{1}{g_m} || R_E + R_S} \tag{5.297}$$

$$= \frac{1}{1 + (1 + g_m R_E) R_S}. \tag{5.298}$$

Since $v_{out}/v_X = g_m R_C$,

$$\frac{v_{out}}{v_{in}} = \frac{1}{1 + (1 + g_m R_E) R_S} \cdot g_m R_C. \tag{5.299}$$

As usual, we have preferred solution by inspection over drawing the small-signal equivalent.

The reader may see a contradiction in our thoughts: on the one hand, we view the low input impedance of the CB stage a *useful* property; on the other hand, we consider the reduction of the input impedance due to R_E *undesirable*. To resolve this apparent contradiction, we must distinguish between the two components $1/g_m$ and R_E, noting that the latter shunts the input

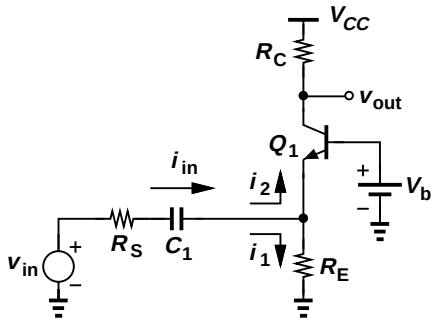


Figure 5.80 Small-signal input current components in a CB stage.

source current to ground, thus "wasting" the signal. As shown in Fig. 5.80, i_{in} splits two ways, with only i_2 reaching R_C and contributing to the output signal. If R_E decreases while $1/g_m$ remains constant, then i_2 also falls.[14] Thus, reduction of R_{in} due to R_E is undesirable. By contrast, if $1/g_m$ decreases while R_E remains constant, then i_2 rises. For R_E to affect the input impedance negligibly, we must have

$$R_E \gg \frac{1}{g_m} \tag{5.300}$$

and hence

$$I_C R_E \gg V_T. \tag{5.301}$$

That is, the dc voltage drop across R_E muts be much greater than V_T.

How is the base voltage, V_b, generated? We can employ a resistive divider similar to that used in the CE stage. Shown in Fig. 5.81(a), such a topology must ensure $I_1 \gg I_B$ to minimize sensitivity to β, yielding

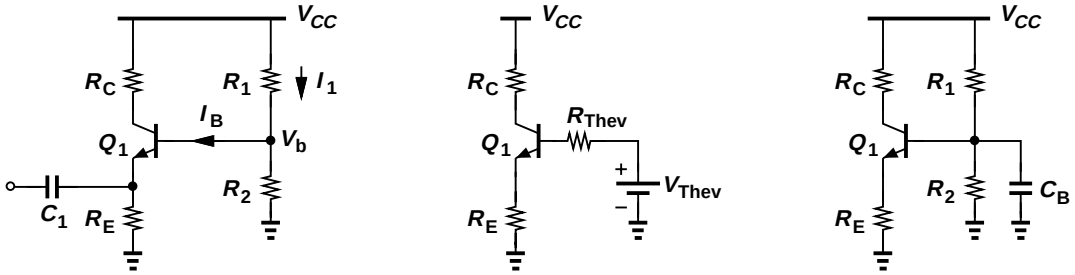


Figure 5.81 (a) CB stage with base bias network, (b) use of Thevenin equivalent, (c) effect of bypass capacitor.

$$V_b \approx \frac{R_2}{R_1 + R_2} V_{CC}. \tag{5.302}$$

However, recall from Eq. (5.286) that a resistance in series with the base *reduces* the voltage gain of the CB stage. Substituting a Thevenin equivalent for R_1 and R_2 as depicted in Fig. 5.81(b),

[14] In the extreme case, $R_E = 0$ (Example 5.41) and $i_2 = 0$.

we recognize that a resistance of $R_{Thev} = R_1||R_2$ now appears in series with the base. For this reason, a "bypass capacitor" is often tied from the base to ground, acting as a short circuit at frequencies of interest [Fig. 5.81(c)].

Example 5.42

Design a CB stage (Fig. 5.82) for a voltage gain of 10 and an input impedance of 50 Ω. Assume $I_S = 5 \times 10^{-16}$ A, $V_A = \infty$, $\beta = 100$, and $V_{CC} = 2.5$ V.

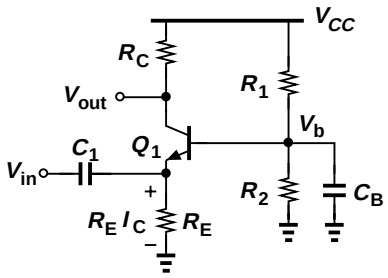


Figure 5.82 Example of CB stage with biasing.

Solution

We begin by selecting $R_E \gg 1/g_m$, e.g., $R_E = 500\ \Omega$, to minimize the undesirable effect of R_E. Thus,

$$R_{in} \approx \frac{1}{g_m} = 50\ \Omega \tag{5.303}$$

and hence

$$I_C = 0.52\ \text{mA}. \tag{5.304}$$

If the base is bypassed to ground

$$A_v = g_m R_C, \tag{5.305}$$

yielding

$$R_C = 500\ \Omega. \tag{5.306}$$

We now determine the base bias resistors. Since the voltage drop across R_E is equal to $500\ \Omega \times 0.52\ \text{mA} = 260$ mV and $V_{BE} = V_T \ln(I_C/I_S) = 899$ mV, we have

$$V_b = I_E R_E + V_{BE} \tag{5.307}$$

$$= 1.16\ \text{V}. \tag{5.308}$$

Selecting the current through R_1 and R_2 to be $10I_B = 52\ \mu$A, we write

$$V_b \approx \frac{R_2}{R_1 + R_2} V_{CC}. \tag{5.309}$$

$$\frac{V_{CC}}{R_1 + R_2} = 52\ \mu\text{A}. \tag{5.310}$$

It follows that

$$R_1 = 25.8\ \text{k}\Omega \tag{5.311}$$

$$R_2 = 22.3\ \text{k}\Omega. \tag{5.312}$$

The last step in the design is to compute the required values of C_1 and C_B according to the signal frequency. For example, if the amplifier is used at the receiver front end of a 900-MHz cellphone, the impedances of C_1 and C_B must be sufficiently small at this frequency. Appearing in series with the emitter of Q_1, C_1 plays a role similar to R_S in Fig. 5.67 and Eq. (5.271). Thus, its impedance, $|C_1\omega|^{-1}$, must remain much less than $1/g_m = 50\ \Omega$. In high-performance applications such as cellphones, we may choose $|C_1\omega|^{-1} = (1/g_m)/20$ to ensure negligible gain degradation. Consequently, for $\omega = 2\pi \times (900\ \text{MHz})$:

$$C_1 = \frac{20 g_m}{\omega} \tag{5.313}$$

$$= 71\ \text{pF}. \tag{5.314}$$

Since the impedance of C_B appears in series with the base and plays a role similar to the term $R_B/(\beta+1)$ in Eq. (5.286), we require that

$$\frac{1}{\beta+1}\left|\frac{1}{C_B\omega}\right| = \frac{1}{20}\frac{1}{g_m} \tag{5.315}$$

and hence

$$C_B = 0.7\ \text{pF}. \tag{5.316}$$

(A common mistake is to make the impedance of C_B negligible with respect to $R_1||R_2$ rather than with respect to $1/g_m$.)

Exercise

Design the above circuit for an input impedance of 100Ω.

5.3.3 Emitter Follower

Another important circuit topology is the emitter follower (also called the "common-collector" stage). The reader is encouraged to review Examples 5.2 - 5.3, rules illustrated in Fig. 5.7, and the possible topologies in Fig. 5.28 before proceeding further. For the sake of brevity, we may also use the term "follower" to refer to emitter followers in this chapter.

Shown in Fig. 5.83, the emitter follower senses the input at the base of the transistor and produces the output at the emitter. The collector is tied to V_{CC} and hence ac ground. We first study the core and subsequently add the biasing elements.

Emitter Follower Core How does the follower in Fig. 5.84(a) respond to a change in V_{in}? If V_{in} rises by a small amount ΔV_{in}, the base-emitter voltage of Q_1 tends to increase, raising the collector and emitter currents. The higher emitter current translates to a greater drop across R_E and hence a *higher* V_{out}. From another perspective, if we assume, for example, V_{out} is constant, then V_{BE} must rise and so must I_E, requiring that V_{out} go up. Since V_{out} changes in the same

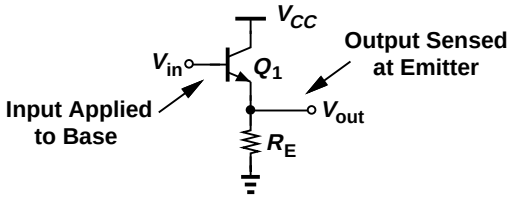
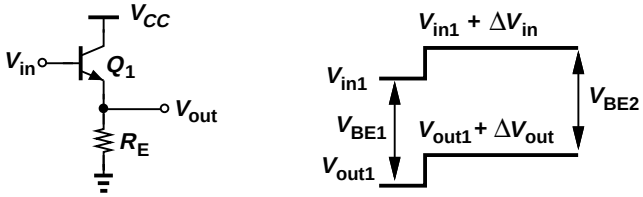


Figure 5.83 Emitter follower.

direction as V_{in}, we expect the voltage gain to be positive. Note that V_{out} is always lower than V_{in} by an amount equal to V_{BE}, and the circuit is said to provide "level shift."



(a) (b)

Figure 5.84 (a) Emitter follower sensing an input change, (b) response of the circuit.

Another interesting and important observation here is that the change in V_{out} cannot be larger than the change in V_{in}. Suppose V_{in} increases from V_{in1} to $V_{in1} + \Delta V_{in}$ and V_{out} from V_{out1} to $V_{out1} + \Delta V_{out}$ [Fig. 5.84(b)]. If the output changes by a *greater* amount than the input, $\Delta V_{out} > \Delta V_{in}$, then V_{BE2} must be *less* than V_{BE1}. But this means the emitter current also decreases and so does $I_E R_E = V_{out}$, contradicting the assumption that V_{out} has increased. Thus, $\Delta V_{out} < \Delta V_{in}$, implying that the follower exhibits a voltage gain less than unity.[15]

The reader may wonder if an amplifier with a subunity gain has any practical value. As explained later, the input and output impedances of the emitter follower make it a particularly useful circuit for some applications.

Let us now derive the small-signal properties of the follower, first assuming $V_A = \infty$. Shown in Fig. 5.85, the equivalent circuit yields

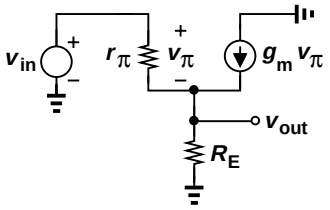


Figure 5.85 Small-signal model of emitter follower.

$$\frac{v_\pi}{r_\pi} + g_m v_\pi = \frac{v_{out}}{R_E} \tag{5.317}$$

and hence

$$v_\pi = \frac{r_\pi}{\beta + 1} \cdot \frac{v_{out}}{R_E}. \tag{5.318}$$

[15] In an extreme case described in Example 5.43, the gain becomes equal to unity.

We also have

$$v_{in} = v_\pi + v_{out}. \tag{5.319}$$

Substituting for v_π from (5.318), we obtain

$$\frac{v_{out}}{v_{in}} = \frac{1}{1 + \dfrac{r_\pi}{\beta+1} \cdot \dfrac{1}{R_E}} \tag{5.320}$$

$$\approx \frac{R_E}{R_E + \dfrac{1}{g_m}}. \tag{5.321}$$

The voltage gain is therefore positive and less than unity.

Example 5.43

In integrated circuits, the follower is typically realized as shown in Fig. 5.86. Determine the voltage gain if the current source is ideal and $V_A = \infty$.

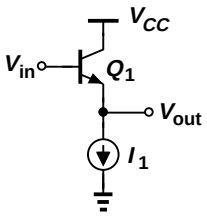


Figure 5.86 Follower with current source.

Solution

Since the emitter resistor is replaced with an ideal current source, the value of R_E in Eq. (5.321) must tend to infinity, yielding

$$A_v = 1. \tag{5.322}$$

This result can also be derived intuitively. A constant current source flowing through Q_1 requires that $V_{BE} = V_T \ln(I_C/I_S)$ remain constant. Writing $V_{out} = V_{in} - V_{BE}$, we recognize that V_{out} exactly *follows* V_{in} if V_{BE} is constant.

Exercise

Repeat the above example if a resistor of value R_1 is placed in series with the collector.

Equation (5.321) suggests that the emitter follower acts as a voltage divider, a perspective that can be reinforced by an alternative analysis. Suppose, as shown in Fig. 5.87(a), we wish to model v_{in} and Q_1 by a Thevenin equivalent. The Thevenin voltage is given by the open-circuit output voltage produced by Q_1 [Fig. 5.87(b)], as if Q_1 operates with $R_E = \infty$ (Example 5.43). Thus, $v_{Thev} = v_{in}$. The Thevenin resistance is obtained by setting the input to zero [Fig. 5.87(c)] and is equal to $1/g_m$. The circuit of Fig. 5.87(a) therefore reduces to that shown in Fig. 5.87(d), confirming operation as a voltage divider.

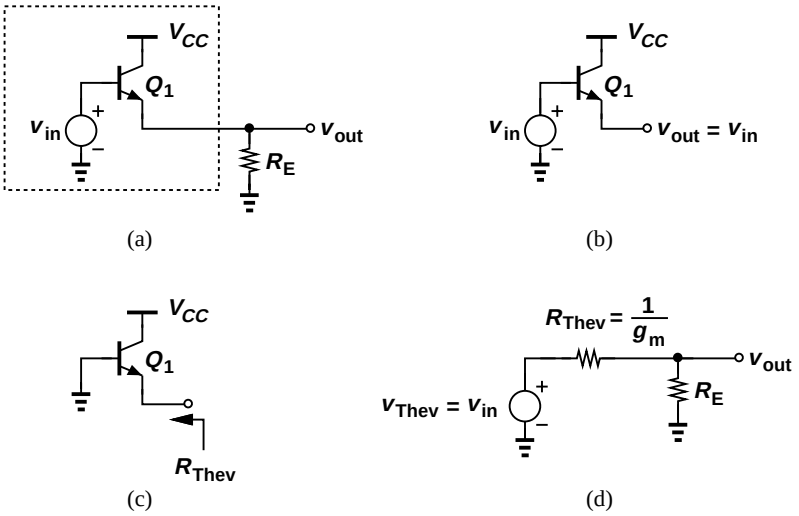


Figure 5.87 (a) Emitter follower stage, (b) Thevenin voltage , (c) Thevenin resistance, (d) simplified circuit.

Example 5.44

Determine the voltage gain of a follower driven by a finite source impedance of R_S [Fig. 5.88(a)] if $V_A = \infty$.

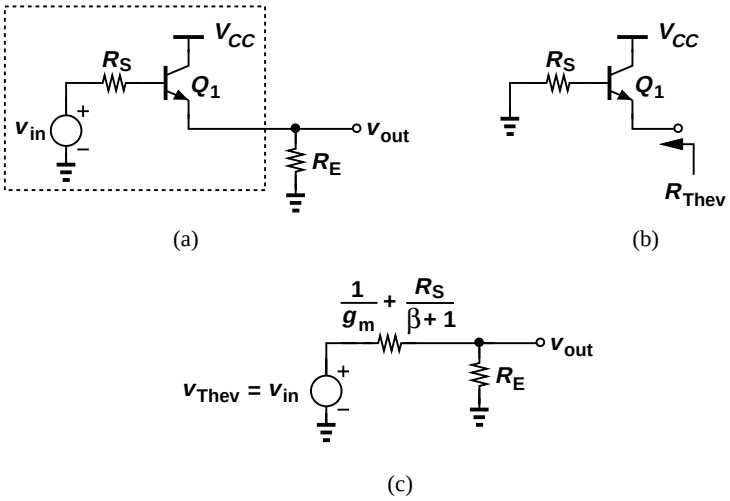


Figure 5.88 (a) Follower with source impedance, (b) Thevenin resistance seen at emitter, (c) simplified circuit.

Solution

We model v_{in}, R_S, and Q_1 by a Thevenin equivalent. The reader can show that the open-circuit voltage is equal to v_{in}. Furthermore, the Thevenin resistance [Fig. 5.88(b)] is given by (5.291) as $R_S/(\beta+1) + 1/g_m$. Figure 5.88(c) depicts the equivalent circuit, revealing that

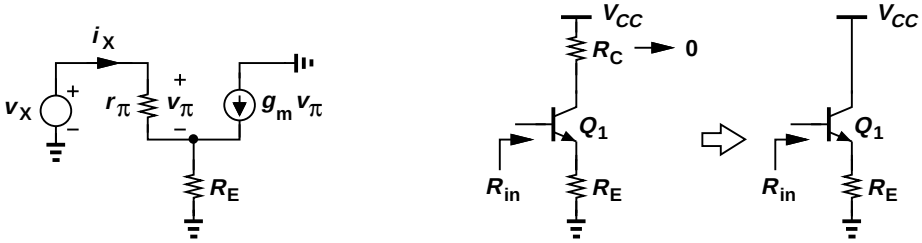
$$\frac{v_{out}}{v_{in}} = \frac{R_E}{R_E + \dfrac{R_S}{\beta+1} + \dfrac{1}{g_m}}. \tag{5.323}$$

This result can also be obtained by solving the small-signal equivalent circuit of the follower.

Exercise

What happens if $R_E = \infty$?

In order to appreciate the usefulness of emitter followers, let us compute their input and output impedances. In the equivalent circuit of Fig. 5.89(a), we have $i_X r_\pi = v_\pi$. Also, the current i_X and $g_m v_\pi$ flow through R_E, producing a voltage drop equal to $(i_X + g_m v_\pi)R_E$. Adding the voltages across r_π and R_E and equating the result to v_X, we have



(a) (b)

Figure 5.89 (a) Input impedance of emitter follower, (b) equivalence of CE and follower stages.

$$v_X = v_\pi + (i_X + g_m v_\pi)R_E \tag{5.324}$$

$$= i_X r_\pi + (i_X + g_m i_X r_\pi)R_E, \tag{5.325}$$

and hence

$$\frac{v_X}{i_X} = r_\pi + (1 + \beta)R_E. \tag{5.326}$$

This expression is identical to that in Eq. (5.162) derived for a degenerated CE stage. This is, of course, no coincidence. Since the input impedance of the CE topology is independent of the collector resistor (for $V_A = \infty$), its value remains unchanged if $R_C = 0$, which is the case for an emitter follower [Fig. 5.89(b)].

The key observation here is that the follower "transforms" the load resistor, R_E, to a much larger value, thereby serving as an efficient "buffer." This concept can be illustrated by an example.

Example 5.45

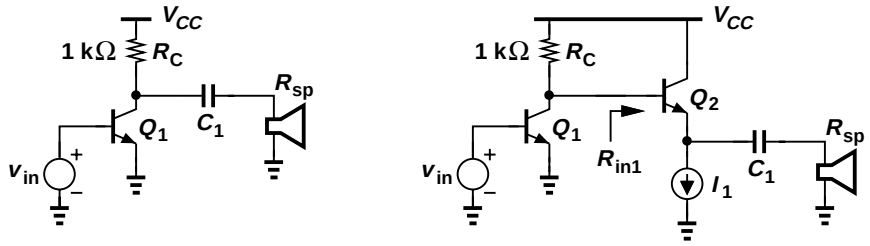
A CE stage exhibits a voltage gain of 20 and an output resistance of 1 kΩ. Determine the voltage gain of the CE amplifier if

(a) The stage drives an 8-Ω speaker directly.

(b) An emitter follower biased at a current of 5 mA is interposed between the CE stage and the speaker. Assume $\beta = 100$, $V_A = \infty$, and the follower is biased with an ideal current source.

Solution

(a) As depicted in Fig. 5.90(a), the equivalent resistance seen at the collector is now given by the parallel combination of R_C and the speaker impedance, R_{sp}, reducing the gain from 20 to $20 \times (R_C || 8\ \Omega)/R_C = 0.159$. The voltage gain therefore degrades drastically.



(a) (b)

Figure 5.90 (a) CE stage and (b) two-stage circuit driving a speaker.

(b) From the arrangement in Fig. 5.90(b), we note that

$$R_{in1} = r_{\pi 2} + (\beta + 1)R_{sp} \tag{5.327}$$

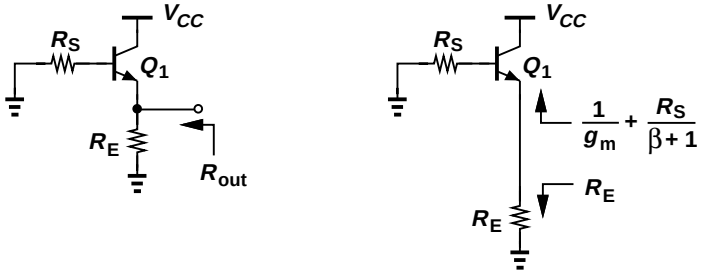
$$= 1058\,\Omega. \tag{5.328}$$

Thus, the voltage gain of the CE stage drops from 20 to $20 \times (R_C||R_{in1})/R_C = 10.28$, a substantial improvement over case (a).

Exercise

Repeat the above example if the emitter follower is biased at a current of 10 mA.

We now calculate the output impedance of the follower, assuming the circuit is driven by a source impedance R_S [Fig. 5.91(a)]. Interestingly, we need not resort to a small-signal model here as R_{out} can be obtained by inspection. As illustrated in Fig. 5.91(b), the output resistance can be viewed as the parallel combination of two components: one seen looking "up" into the emitter and another looking "down" into R_E. From Fig. 5.88, the former is equal to $R_S/(\beta + 1) + 1/g_m$, and hence



(a) (b)

Figure 5.91 (a) Output impedance of a follower, (b) components of output resistance.

$$R_{out} = \left(\frac{R_S}{\beta + 1} + \frac{1}{g_m}\right)||R_E. \tag{5.329}$$

This result can also be derived from the Thevenin equivalent shown in Fig. 5.88(c) by setting v_{in} to zero.

Equation (5.329) reveals another important attribute of the follower: the circuit transforms the source impedance, R_S, to a much lower value, thereby providing higher "driving" capability. We say the follower operates as a good "voltage buffer" because it displays a high input impedance (like a voltmeter) and a low output impedance (like a voltage source).

Effect of Transistor Output Resistance Our analysis of the follower has thus far neglected the Early effect. Fortunately, the results obtained above can be readily modified to reflect this nonideality. Figure 5.92 illustrates a key point that facilitates the analysis: in small-signal operation, r_O appears in parallel with R_E. We can therefore rewrite Eqs. (5.323), (5.326) and (5.329) as

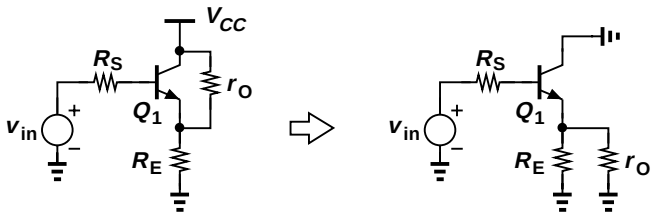


Figure 5.92 Follower including transistor output resistance.

$$A_v = \frac{R_E||r_O}{R_E||r_O + \dfrac{R_S}{\beta+1} + \dfrac{1}{g_m}} \tag{5.330}$$

$$R_{in} = r_\pi + (\beta+1)(R_E||r_O) \tag{5.331}$$

$$R_{out} = \left(\frac{R_S}{\beta+1} + \frac{1}{g_m}\right)||R_E||r_O. \tag{5.332}$$

Example 5.46

Determine the small-signal properties of an emitter follower using an ideal current source (as in Example 5.43) but with a finite source impedance R_S.

Solution

Since $R_E = \infty$, we have

$$A_v = \frac{r_O}{r_O + \dfrac{R_S}{\beta+1} + \dfrac{1}{g_m}} \tag{5.333}$$

$$R_{in} = r_\pi + (\beta+1)r_O) \tag{5.334}$$

$$R_{out} = \left(\frac{R_S}{\beta+1} + \frac{1}{g_m}\right)||r_O. \tag{5.335}$$

Also, $g_m r_O \gg 1$, and hence

$$A_v \approx \frac{r_O}{r_O + \dfrac{R_S}{\beta+1}} \tag{5.336}$$

$$R_{in} \approx (\beta+1)r_O. \tag{5.337}$$

We note that A_v approaches unity if $R_S \ll (\beta+1)r_O$, a condition typically valid.

Exercise

How are the results modified if $R_E < \infty$?

The buffering capability of followers is sometimes attributed to their "current gain." Since a base current i_B results in an emitter current of $(\beta+1)i_B$, we can say that for a current i_L delivered to the load, the follower draws only $i_L/(\beta+1)$ from the source voltage (Fig. 5.93). Thus, v_X sees the load impedance multiplied by $(\beta+1)$.

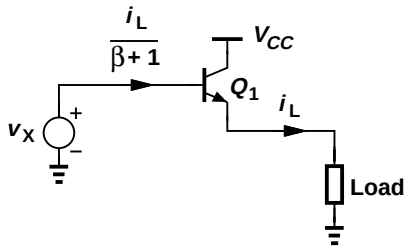


Figure 5.93 Current amplification in a follower.

Emitter Follower with Biasing The biasing of emitter followers entails defining both the base voltage and the collector (emitter) current. Figure 5.94(a) depicts an example similar to the scheme illustrated in Fig. 5.19 for the CE stage. As usual, the current flowing through R_1 and R_2 is chosen to be much greater than the base current.

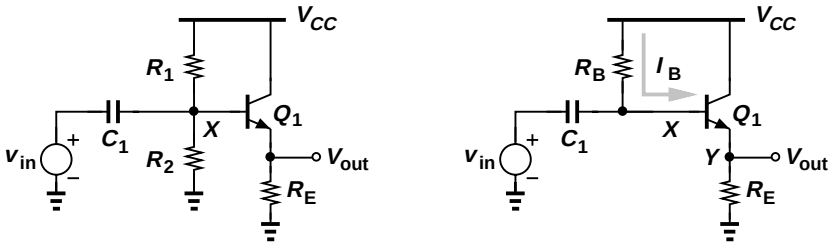


Figure 5.94 Biasing a follower by means of (a) resistive divider, (b) single base resistor.

It is interesting to note that, unlike the CE topology, the emitter follower can operate with a base voltage near V_{CC}. This is because the collector is tied to V_{CC}, allowing the same voltage for the base without driving Q_1 into saturation. For this reason, followers are often biased as shown in Fig. 5.94(b), where $R_B I_B$ is chosen much less than the voltage drop across R_E, thus lowering the sensitivity to β. The following example illustrates this point.

Example 5.47

The follower of Fig. 5.94(b) employs $R_B = 10\ \text{k}\Omega$ and $R_E = 1\ \text{k}\Omega$. Calculate the bias current and voltages if $I_S = 5 \times 10^{-16}$ A, $\beta = 100$, and $V_{CC} = 2.5$ V. What happens if β drops to 50?

Solution

To determine the bias current, we follow the iterative procedure described in Section 5.2.3. Writ-

ing a KVL through R_B, the base-emitter junction, and R_E gives

$$\frac{R_B I_C}{\beta} + V_{BE} + R_E I_C = V_{CC}, \tag{5.338}$$

which, with $V_{BE} \approx 800$ mV, leads to

$$I_C = 1.545 \text{ mA}. \tag{5.339}$$

It follows that $V_{BE} = V_T \ln(I_C/I_S) = 748$ mV. Using this value in Eq. (5.338), we have

$$I_C = 1.593 \text{ mA}, \tag{5.340}$$

a value close to that in (5.339) and hence relatively accurate. Under this condition, $I_B R_B = 159$ mV whereas $R_E I_C = 1.593$ V.

Since $I_B R_B \ll R_E I_C$, we expect that variation of β and hence $I_B R_B$ negligibly affects the voltage drop across R_E and hence the emitter and collector currents. As a rough estimate, for $\beta = 50$, $I_B R_B$ is doubled (≈ 318 mV), reducing the drop across R_E by 159 mV. That is, $I_E = (1.593 \text{ V} - 0.159 \text{ V})/1 \text{ k}\Omega = 1.434$ mA, implying that a twofold change in β leads to a 10% change in the collector current. The reader is encouraged to repeat the above iterations with $\beta = 50$ and determine the exact current.

Exercise

If R_B is doubled, is the circuit more or less sensitive to the variation in β?

As manifested by Eq. (5.338), the topologies of Fig. 5.94 suffer from supply-dependent biasing. In integrated circuits, this issue is resolved by replacing the emitter resistor with a constant current source (Fig. 5.95). Now, since I_{EE} is constant, so are V_{BE} and $R_B I_B$. Thus, if V_{CC} rises, so do V_X and V_Y, but the bias current remains constant.

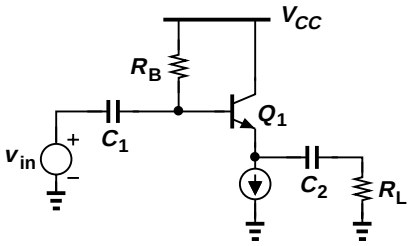


Figure 5.95 Capacitive coupling at input and output of a follower.

5.4 Summary and Additional Examples

This chapter has created a foundation for amplifier design, emphasizing that a proper bias point must be established to define the small-signal properties of each circuit. Depicted in Fig. 5.96, the three amplifier topologies studied here exhibit different gains and I/O impedances, each serving a specific application. CE and CB stages can provide a voltage gain greater than unity and their input and output impedances are independent of the load and source impedances, respectively (if

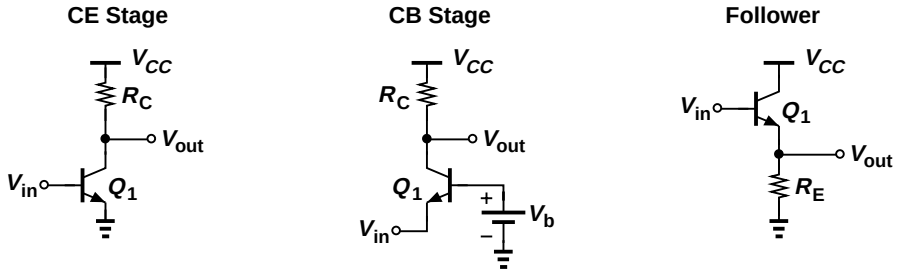


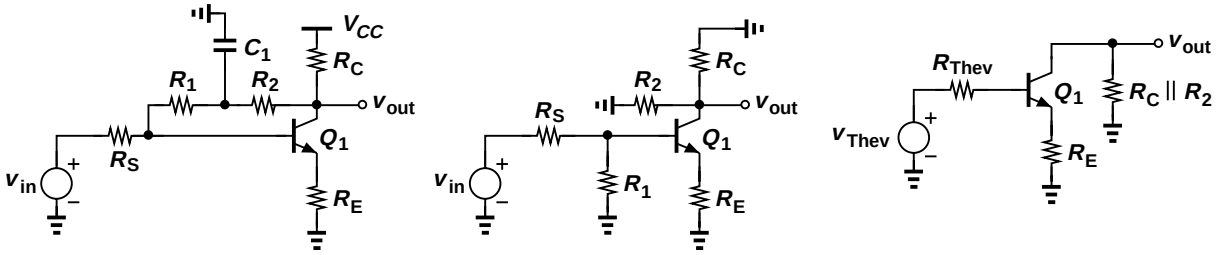
Figure 5.96 Summary of bipolar amplifier topologies.

$V_A = \infty$). On the other hand, followers display a voltage gain of at most unity but their terminal impedances depend on the load and source impedances.

In this section, we consider a number of challenging examples, seeking to improve our circuit analysis techniques. As usual, our emphasis is on solution by inspection and hence intuitive understanding of the circuits. We assume various capacitors used in each circuit have a negligible impedance at the signal frequencies of interest.

Example 5.48

Assuming $V_A = \infty$, determine the voltage gain of the circuit shown in Fig. 5.97(a).



(a) (b) (c)

Figure 5.97 (a) Example of CE stage, (b) equivalent circuit with C_1 shorted, (c) simplified circuit .

Solution

The simplified ac model is depicted in Fig. 5.97(b), revealing that R_1 appears between base and ground, and R_2 between collector and ground. Replacing v_{in}, R_S, and R_1 with a Thevenin equivalent [Fig. 5.97(c)], we have

$$v_{Thev} = \frac{R_1}{R_1 + R_S} v_{in} \tag{5.341}$$

$$R_{Thev} = R_1 || R_S. \tag{5.342}$$

The resulting circuit resembles that in Fig. 5.43(a) and satisfies Eq. (5.185):

$$\frac{v_{out}}{v_{Thev}} = -\frac{R_2 || R_C}{\dfrac{R_{Thev}}{\beta + 1} + \dfrac{1}{g_m} + R_E}. \tag{5.343}$$

Substituting for v_{Thev} and R_{Thev} gives

$$\frac{v_{out}}{v_{in}} = -\frac{R_2||R_C}{\dfrac{R_1||R_S}{\beta+1} + \dfrac{1}{g_m} + R_E} \cdot \frac{R_1}{R_1+R_S}. \tag{5.344}$$

Exercise

What happens if a very large capacitor is added from the emitter of Q_1 to ground?

Example 5.49

Assuming $V_A = \infty$, compute the voltage gain of the circuit shown in Fig. 5.98(a).

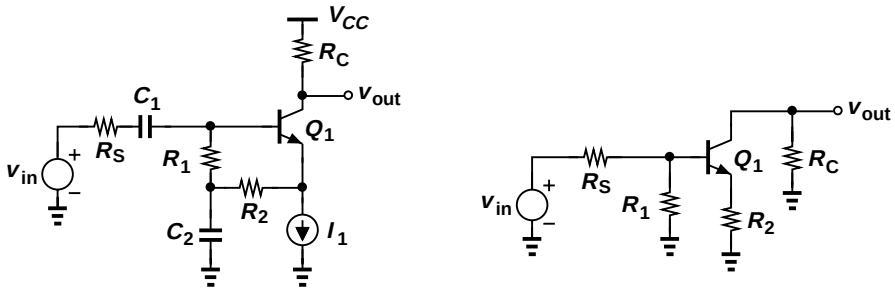


Figure 5.98 (a) Example of CE stage, (b) simplified circuit.

Solution

As shown in the simplified diagram of Fig. 5.98(b), R_2 appears as an emitter degeneration resistor. As in the above example, we replace v_{in}, R_S, and R_1 with a Thevenin equivalent and utilize Eq. (5.185):

$$\frac{v_{out}}{v_{in}} = -\frac{R_C}{\dfrac{R_{Thev}}{\beta+1} + \dfrac{1}{g_m} + R_2} \tag{5.345}$$

and hence

$$\frac{v_{out}}{v_{in}} = -\frac{R_C}{\dfrac{R_S||R_1}{\beta+1} + \dfrac{1}{g_m} + R_2} \cdot \frac{R_1}{R_1+R_S}. \tag{5.346}$$

Exercise

What happens if C_2 is tied from the emitter of Q_1 to ground?

Example 5.50

Assuming $V_A = \infty$, compute the voltage gain and input impedance of the circuit shown in Fig. 5.99(a).

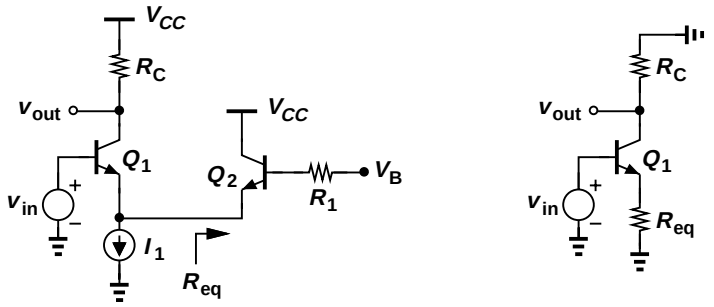


Figure 5.99 (a) Example of CE stage, (b) simplified circuit.

Solution

The circuit resembles a CE stage (why?) degenerated by the impedance seen at the emitter of Q_2, R_{eq}. Recall from Fig. 5.75 that

$$R_{eq} = \frac{R_1}{\beta+1} + \frac{1}{g_{m2}}. \tag{5.347}$$

The simplified model in Fig. 5.99(b) thus yields

$$A_v = \frac{-R_C}{\dfrac{1}{g_{m1}} + R_{eq}} \tag{5.348}$$

$$= \frac{-R_C}{\dfrac{1}{g_{m1}} + \dfrac{R_1}{\beta+1} + \dfrac{1}{g_{m2}}}. \tag{5.349}$$

The input impedance is also obtained from Fig. 5.75:

$$R_{in} = r_{\pi 1} + (\beta+1)R_{eq} \tag{5.350}$$

$$= r_{\pi 1} + R_1 + r_{\pi 2}. \tag{5.351}$$

Exercise

Repeat the above example if R_1 is placed in series with the emitter of Q_2.

Example 5.51

Calculate the voltage gain of the circuit in Fig. 5.100(a) if $V_A = \infty$.

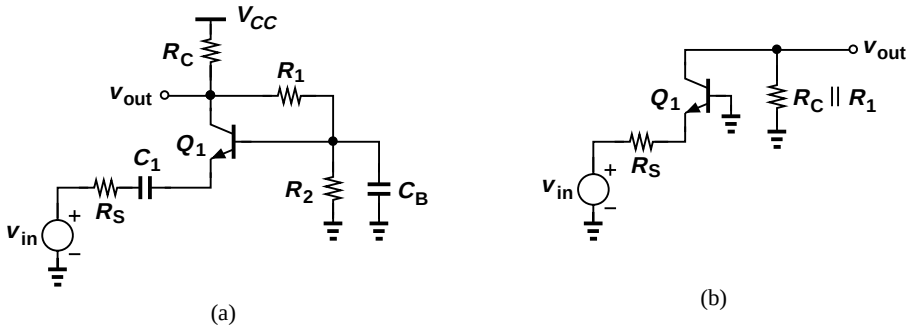


Figure 5.100 (a) Example of CB stage, (b) simplified circuit.

Solution

Since the base is at ac ground, R_1 appears in parallel with R_C and R_2 is shorted to ground on both ends [Fig. 5.100(b)]. The voltage gain is given by (5.271), but with R_C replaced by $R_C||R_1$:

$$A_v = \frac{R_C||R_1}{R_S + \dfrac{1}{g_m}}. \tag{5.352}$$

Exercise

What happens if R_C is replaced by an ideal currents source?

Example 5.52

Determine the input impedance of the circuit shown in Fig. 5.101(a) if $V_A = \infty$.

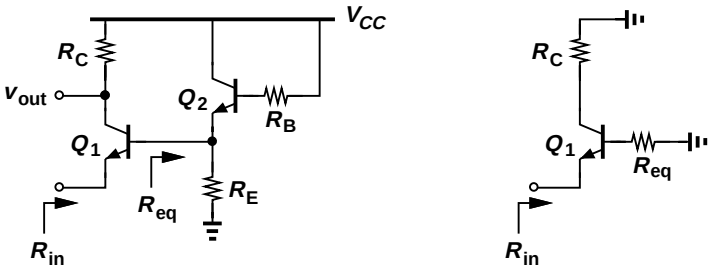


Figure 5.101 (a) Example of CB stage, (b) simplified circuit.

Solution

In this circuit, Q_1 operates as a common-base device (why?) but with a resistance R_{eq} in series with its base [Fig. 5.101(b)]. To obtain R_{eq}, we recognize that Q_2 resembles an emitter follower, e.g., the topology in Fig. 5.91(a), concluding that R_{eq} can be viewed as the output resistance of such a stage, as given by Eq. (5.329):

$$R_{eq} = \left(\frac{R_B}{\beta + 1} + \frac{1}{g_{m2}}\right) ||R_E. \tag{5.353}$$

Now, from Fig. 5.101(b), we observe that R_{in} contains two components: one equal to the resistance in series with the base, R_{eq}, divided by $\beta+1$, and another equal to $1/g_{m1}$:

$$R_{in} = \frac{R_{eq}}{\beta+1} + \frac{1}{g_{m1}} \tag{5.354}$$

$$= \frac{1}{\beta+1}\left[\left(\frac{R_B}{\beta+1} + \frac{1}{g_{m2}}\right) || R_E\right] + \frac{1}{g_{m1}}. \tag{5.355}$$

The reader is encouraged to obtain R_{in} through a complete small-signal analysis and compare the required "manual labor" to the above algebra.

Exercise

What happens if the current gain of Q_2 goes to infinity?

Example 5.53

Compute the voltage gain and the output impedance of the circuit depicted in Fig. 5.102(a) with $V_A < \infty$.

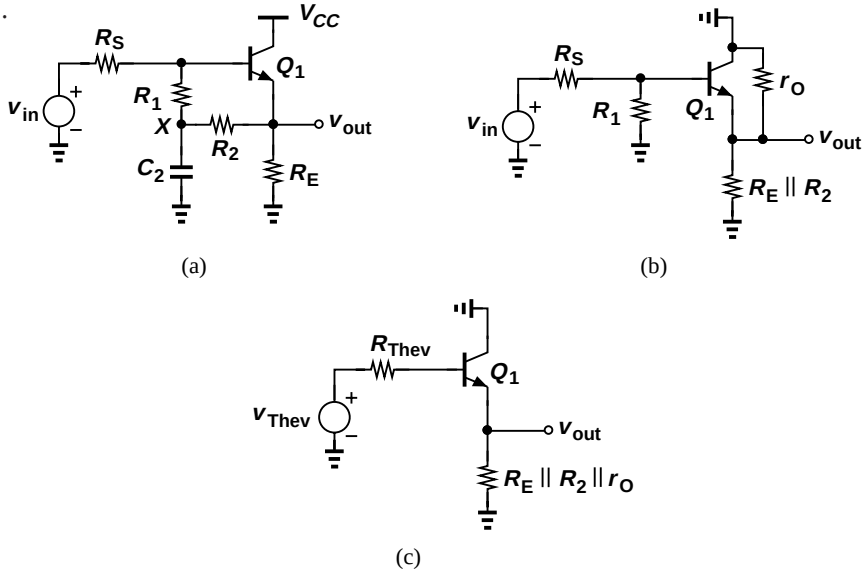


Figure 5.102 (a) Example of emitter follower, (b) circuit with C_1 shorted, (c) simplified circuit.

Solution

Noting that X is at ac ground, we construct the simplified circuit shown in Fig. 5.102(b), where the output resistance of Q_1 is explicitly drawn. Replacing v_{in}, R_S, and R_1 with their Thevenin equivalent and recognizing that R_E, R_2, and r_O appear in parallel [Fig. 5.102(c)], we employ Eq. (5.330) and write

$$\frac{v_{out}}{v_{Thev}} = \frac{R_E||R_2||r_O}{R_E||R_2||r_O + \dfrac{1}{g_m} + \dfrac{R_{Thev}}{\beta+1}} \tag{5.356}$$

and hence

$$\frac{v_{out}}{v_{in}} = \frac{R_E||R_2||r_O}{R_E||R_2||r_O + \dfrac{1}{g_m} + \dfrac{R_S||R_1}{\beta+1}} \cdot \frac{R_1}{R_1+R_S}. \tag{5.357}$$

For the output resistance, we refer to Eq. (5.332):

$$R_{out} = \left(\frac{R_{Thev}}{\beta+1} + \frac{1}{g_m}\right) ||(R_E||R_2||r_O) \tag{5.358}$$

$$= \left(\frac{R_S||R_1}{\beta+1} + \frac{1}{g_m}\right) ||R_E||R_2||r_O. \tag{5.359}$$

Exercise

What happens if $R_S = 0$?

Example 5.54

Determine the voltage gain and I/O impedances of the topology shown in Fig. 5.103(a). Assume $V_A = \infty$ and equal β's for npn and pnp transistors.

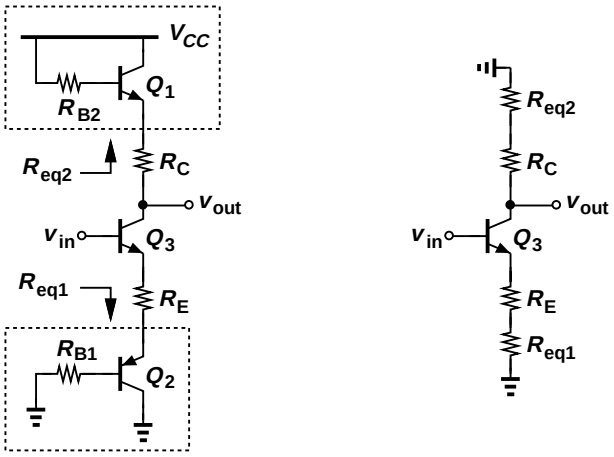


Figure 5.103 (a) Example of CE stage, (b) simplified circuit.

Solution

We identify the stage as a CE amplifier with emitter degeneration and a composite collector load. As the first step, we represent the role of Q_2 and Q_3 by the impedances that they create at their emitter. Since R_{eq1} denotes the impedance seen looking into the emitter of Q_2 with a base resistance of R_{B1}, we have from Fig. 5.75

$$R_{eq1} = \frac{R_{B1}}{\beta+1} + \frac{1}{g_{m2}}. \tag{5.360}$$

Similarly,

$$R_{eq2} = \frac{R_{B2}}{\beta+1} + \frac{1}{g_{m1}}, \tag{5.361}$$

leading to the simplified circuit shown in Fig. 5.103(b). It follows that

$$A_v = -\frac{R_C + R_{eq2}}{R_{eq1} + \dfrac{1}{g_{m3}} + R_E} \tag{5.362}$$

$$= -\frac{R_C + \dfrac{R_{B2}}{\beta+1} + \dfrac{1}{g_{m1}}}{\dfrac{R_{B1}}{\beta+1} + \dfrac{1}{g_{m2}} + \dfrac{1}{g_{m3}} + R_E}. \tag{5.363}$$

Also,

$$R_{in} = r_{\pi 3} + (\beta+1)(R_E + R_{eq1}) \tag{5.364}$$

$$= r_{\pi 3} + (\beta+1)\left(R_E + \frac{R_{B1}}{\beta+1} + \frac{1}{g_{m2}}\right), \tag{5.365}$$

and

$$R_{out} = R_C + R_{eq2} \tag{5.366}$$

$$= R_C + \frac{R_{B2}}{\beta+1} + \frac{1}{g_{m1}}. \tag{5.367}$$

Exercise

What happens if $R_{B2} \to \infty$?

5.5 Chapter Summary

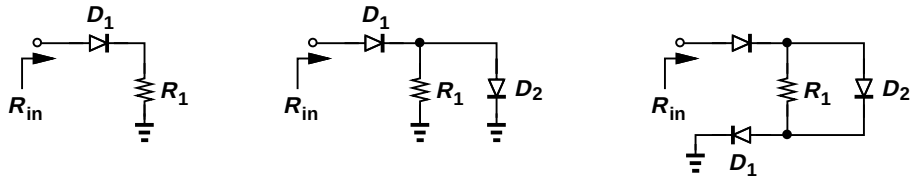
- In addition to gain, the input and output impedances of amplifiers determine the ease with which various stages can be cascaded.
- Voltage amplifiers must ideally provide a high input impedance (so that they can sense a voltage without disturbing the node) and a low output impedance (so that they can drive a load without reduction in gain).
- The impedances seen looking into the base, collector, and emitter of a bipolar transistor are equal to r_π (with emitter grounded), r_O (with emitter grounded), and $1/g_m$ (with base grounded), respectively.
- In order to obtain the required small-signal bipolar device parameters such as g_m, r_π, and r_O, the transistor must be "biased," i.e., carry a certain collector current and operate in the active region. Signals simply perturb these conditions.
- Biasing techniques establish the required base-emitter and base-collector voltages while providing the base current.

- With a single bipolar transistor, only three amplifier topologies are possible: common-emitter and common-base stages and emitter followers.
- The CE stage provides a moderate voltage gain, a moderate input impedance, and a moderate output impedance.
- Emitter degeneration improves the linearity but lowers the voltage gain.
- Emitter degeneration raises the output impedance of CE stages considerably.
- The CB stage provides a moderate voltage gain, a low input impedance, and a moderate output impedance.
- The voltage gain expressions for CE and CB stages are similar but for a sign.
- The emitter follower provides a voltage gain less than unity, a high input impedance, and a low output impedance, serving as a good voltage buffer.

Problems

1. An antenna can be modeled as a Thevenin equivalent having a sinusoidal voltage source $V_0 \cos \omega t$ and an output resistance R_{out}. Determine the average power delivered to a load resistance R_L and plot the result as a function of R_L.

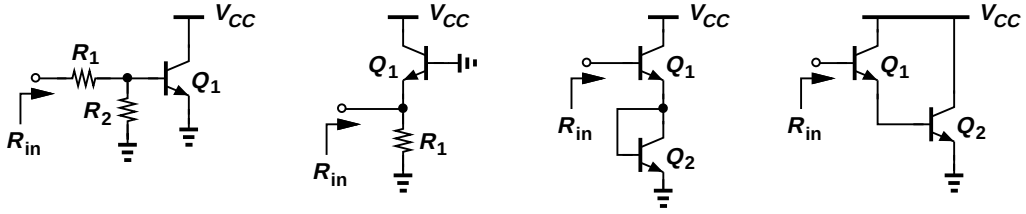
2. Determine the small-signal input resistance of the circuits shown in Fig. 5.104. Assume all diodes are forward-biased. (Recall from Chapter 3 that each diode behaves as a linear resistance if the voltage and current changes are small.)



(a) (b) (c)

Figure 5.104

3. Compute the input resistance of the circuits depicted in Fig. 5.105. Assume $V_A = \infty$.



(a) (b) (c) (d)

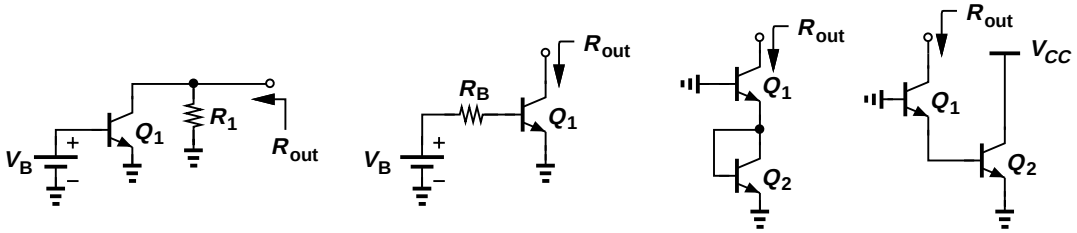
Figure 5.105

4. Compute the output resistance of the circuits depicted in Fig. 5.106.

5. Determine the input impedance of the circuits depicted in Fig. 5.107. Assume $V_A = \infty$.

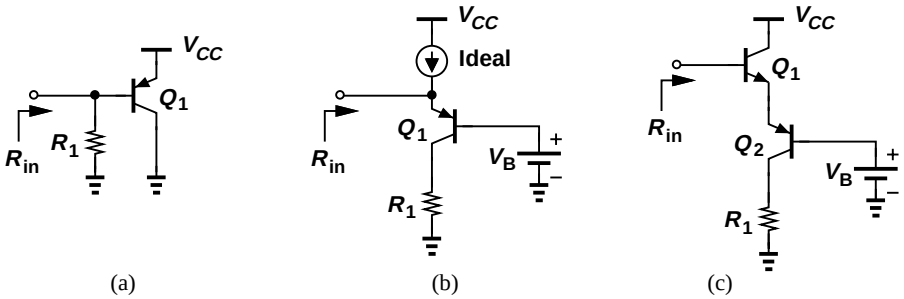
6. Compute the output impedance of the circuits shown in Fig. 5.108.

7. Compute the bias point of the circuits depicted in Fig. 5.109. Assume $\beta = 100$, $I_S =$

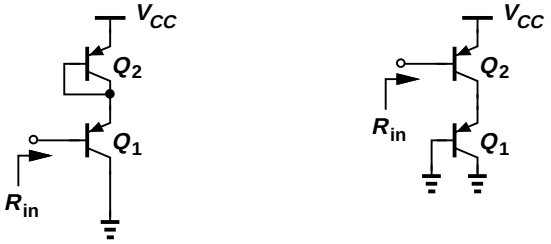


(a) (b) (c) (d)

Figure 5.106

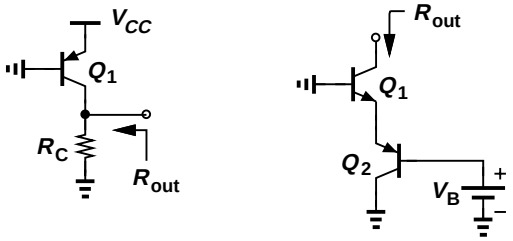


(a) (b) (c)



(d) (e)

Figure 5.107



(a) (b)

Figure 5.108

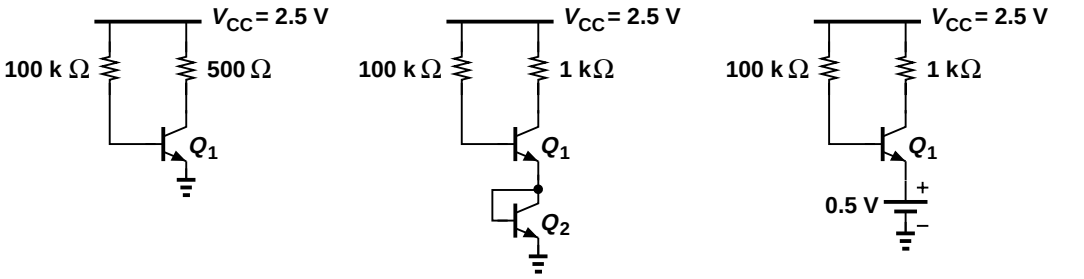
6×10^{-16} A, and $V_A = \infty$.

8. Construct the small-signal equivalent of each of the circuits in Problem 7.

9. Calculate the bias point of the circuits shown in Fig. 5.110. Assume $\beta = 100$, $I_S = 5 \times 10^{-16}$ A, and $V_A = \infty$.

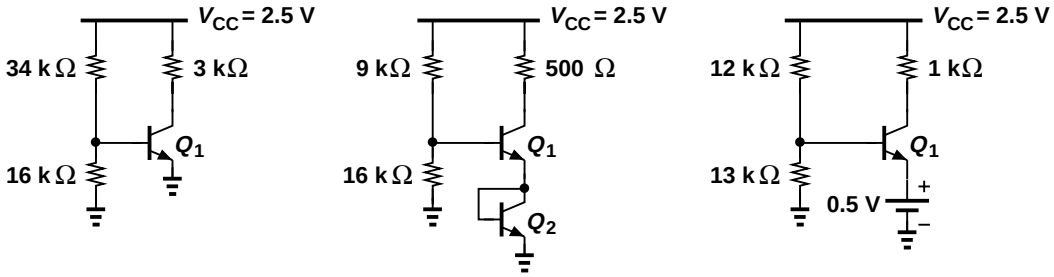
10. Construct the small-signal equivalent of each of the circuits in Problem 9.

11. Consider the circuit shown in Fig. 5.111, where $\beta = 100$, $I_S = 6 \times 10^{-16}$ A, and $V_A = \infty$.



(a) (b) (c)

Figure 5.109



(a) (b) (c)

Figure 5.110

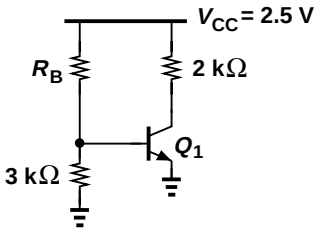


Figure 5.111

(a) What is the minimum value of R_B that guarantees operation in the active mode?
(b) With the value found in R_B, how much base-collector forward bias is sustained if β rises to 200?

12. In the circuit of Fig. 5.112, $\beta = 100$ and $V_A = \infty$.

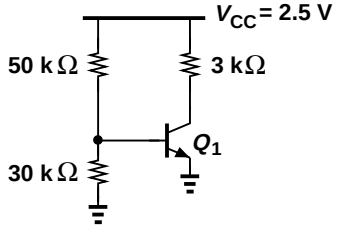


Figure 5.112

(a) If the collector current of Q_1 is equal to 0.5 mA, calculate the value of I_S.

(b) If Q_1 is biased at the edge of saturation, calculate the value of I_S.

13. The circuit of Fig. 5.113 must be designed for an input impedance of greater than 10 kΩ and

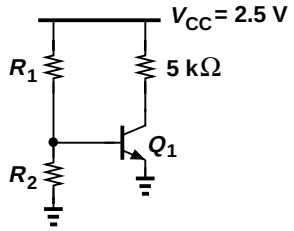


Figure 5.113

a g_m of at least $1/(260\,\Omega)$. If $\beta = 100$, $I_S = 2 \times 10^{-17}$ A, and $V_A = \infty$, determine the minimum allowable values of R_1 and R_2.

14. Repeat Problem 13 for a g_m of at least $1/(26\,\Omega)$. Explain why no solution exists.

15. We wish to design the CE stage depicted in Fig. 5.114 for a gain ($= g_m R_C$) of A_0 with an

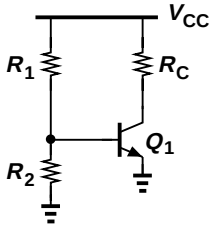


Figure 5.114

output impedance of R_0. What is the maximum achievable input impedance here? Assume $V_A = \infty$.

16. The circuit of Fig. 5.115 is designed for a collector current of 0.25 mA. Assume $I_S =$

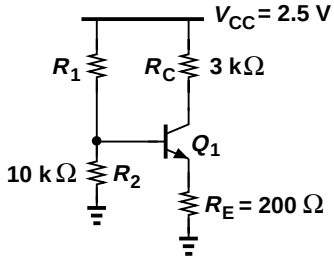


Figure 5.115

6×10^{-16} A, $\beta = 100$, and $V_A = \infty$.
(a) Determine the required value of R_1.
(b) What is the error in I_C if R_E deviates from its nominal value by 5%?

17. In the circuit of Fig. 5.116, determine the maximum value of R_2 that guarantees operation of Q_1 in the active mode. Assume $\beta = 100$, $I_S = 10^{-17}$ A, and $V_A = \infty$.

18. Consider the circuit shown in Fig. 5.117, where $I_{S1} = 2I_{S2} = 5 \times 10^{-16}$ A, $\beta_1 = \beta_2 = 100$, and $V_A = \infty$.
(a) Determine the collector currents of Q_1 and Q_2.
(b) Construct the small-signal equivalent circuit.

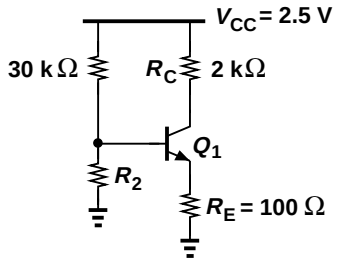


Figure 5.116

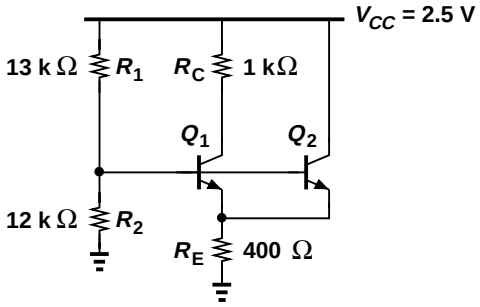


Figure 5.117

19. In the circuit depicted in Fig. 5.118, $I_{S1} = I_{S2} = 4 \times 10^{-16}$ A, $\beta_1 = \beta_2 = 100$, and $V_A = \infty$.

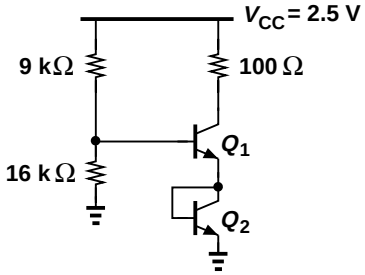


Figure 5.118

(a) Determine the operating point of the transistor.
(b) Draw the small-signal equivalent circuit.

20. The circuit of Fig. 5.119 must be biased with a collector current of 1 mA. Compute the

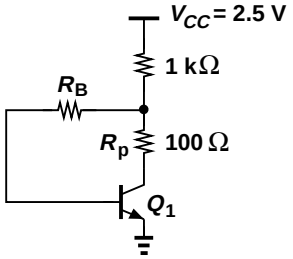


Figure 5.119

required value of R_B if $I_S = 3 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

21. In the circuit of Fig. 5.120, $V_X = 1.1$ V. If $\beta = 100$ and $V_A = \infty$, what is the value of I_S?

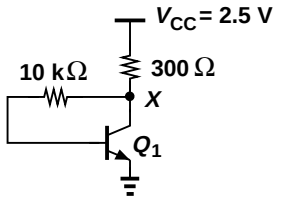


Figure 5.120

22. Consider the circuit shown in Fig. 5.121, where $I_S = 6 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$. Calculate the operating point of Q_1.

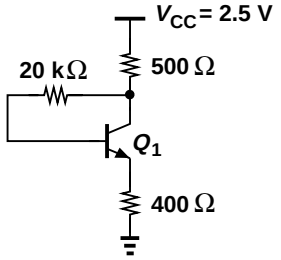


Figure 5.121

23. Due to a manufacturing error, a parasitic resistor, R_P, has appeared in series with the collector of Q_1 in Fig. 5.122. What is the minimum allowable value of R_B if the base-collector

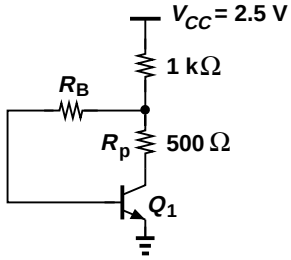


Figure 5.122

forward bias must not exceed 200 mV? Assume $I_S = 3 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

24. In the circuit of Fig. 5.123, $I_S = 8 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

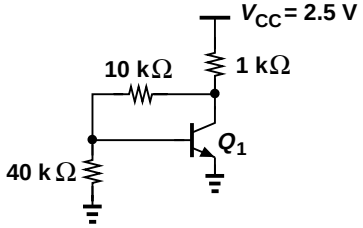


Figure 5.123

(a) Determine the operating point of Q_1.

(b) Draw the small-signal equivalent circuit.

25. In the circuit of Fig. 5.124, $I_{S1} = I_{S2} = 3 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

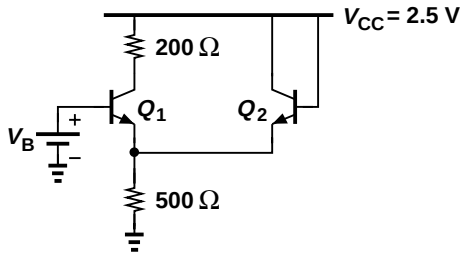
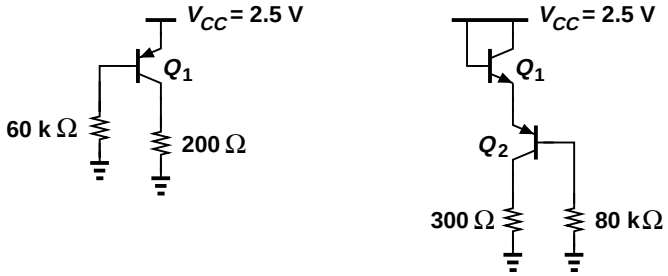


Figure 5.124

(a) Calculate V_B such that Q_1 carries a collector current of 1 mA.
(b) Construct the small-signal equivalent circuit.

26. Determine the bias point of each circuit shown in Fig. 5.125. Assume $\beta_{npn} = 2\beta_{pnp} = 100$,



(a) (b)

Figure 5.125

$I_S = 9 \times 10^{-16}$ A, and $V_A = \infty$.

27. Construct the small-signal model of the circuits in Problem 26.

28. Calculate the bias point of the circuits shown in Fig. 5.126. Assume $\beta_{npn} = 2\beta_{pnp} = 100$,

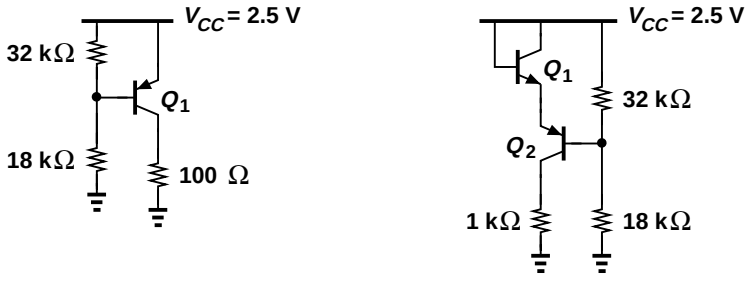


Figure 5.126 (a) (b)

$I_S = 9 \times 10^{-16}$ A, and $V_A = \infty$.

29. Draw the small-signal model of the circuits in Problem 28.

30. We have chosen R_B in Fig. 5.127 to place Q_1 at the edge of saturation. But the actual value of this resistor can vary by $\pm 5\%$. Determine the forward- or reverse-bias across the base-collector junction at these two extremes. Assume $\beta = 50$, $I_S = 8 \times 10^{-16}$ A, and $V_A = \infty$.

31. Calculate the value of R_E in Fig. 5.128 such that Q_1 sustains a reverse bias of 300 mV

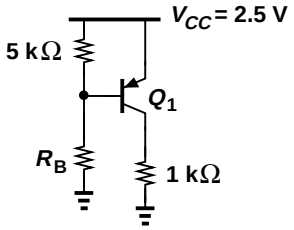


Figure 5.127

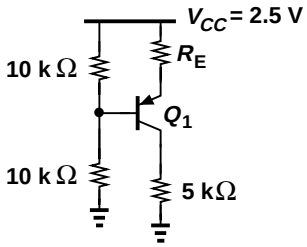


Figure 5.128

across its base-collector junction. Assume $\beta = 50$, $I_S = 8 \times 10^{-16}$ A, and $V_A = \infty$. What happens if the value of R_E is halved?

32. If $\beta = 80$ and $V_A = \infty$, what value of I_S yields a collector current of 1 mA in Fig. 5.129?

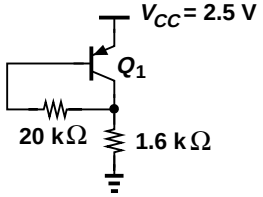
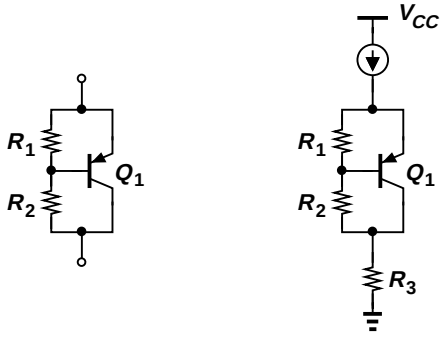


Figure 5.129

33. The topology depicted in Fig. 5.130(a) is called a "V_{BE} multiplier."(The npn counterpart has a similar topology.) Constructing the circuit shown in Fig. 5.130(b), determine the collector-



(a) (b)

Figure 5.130

emitter voltage of Q_1 if the base current is negligible. (The npn counterpart can also be used.)

34. We wish to design the CE stage of Fig. 5.131 for a voltage gain of 20. What is the minimum

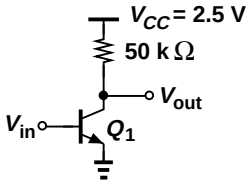


Figure 5.131

allowable supply voltage if Q_1 must remain in the active mode? Assume $V_A = \infty$ and $V_{BE} = 0.8$ V.

35. The circuit of Fig. 5.132 must be designed for maximum voltage gain while maintaining Q_1

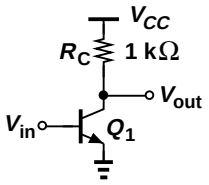


Figure 5.132

in the active mode. If $V_A = 10$ V and $V_{BE} = 0.8$ V, calculate the required bias current.

36. The CE stage of Fig. 5.133 employs an ideal current source as the load. If the voltage gain

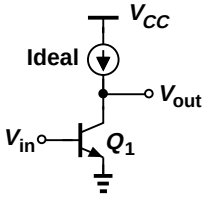


Figure 5.133

is equal to 50 and the output impedance equal to 10 kΩ, determine the bias current of the transistor.

37. Suppose the bipolar transistor in Fig. 5.134 exhibits the following hypothetical characteris-

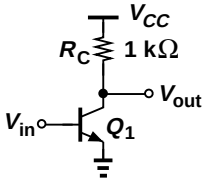


Figure 5.134

tic:

$$I_C = I_S \exp \frac{V_{BE}}{2V_T}, \tag{5.368}$$

and no Early effect. Compute the voltage gain for a bias current of 1 mA.

38. Determine the voltage gain and I/O impedances of the circuits shown in Fig. 5.135. Assume $V_A = \infty$. Transistor Q_2 in Figs. 5.135(d) and (e) operates in soft saturation.

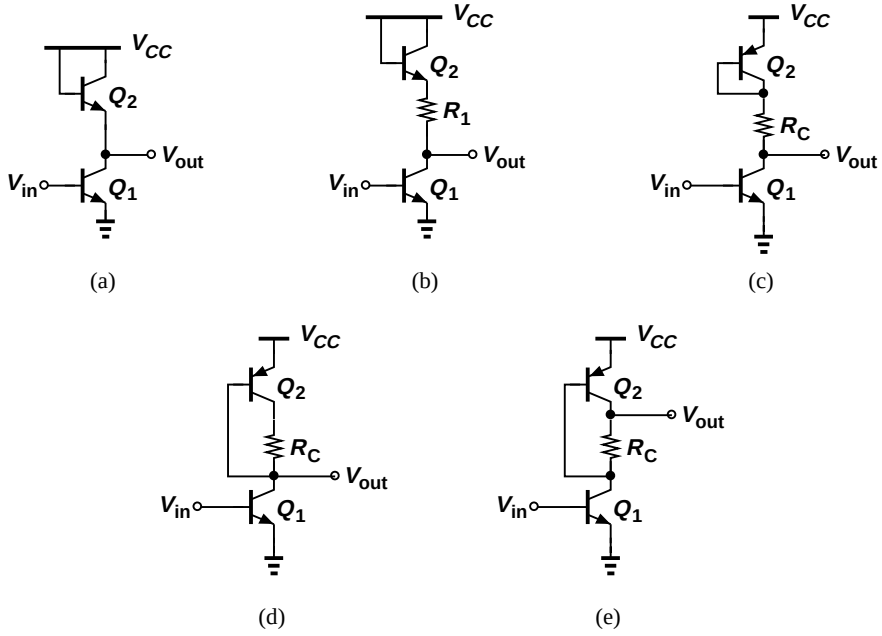


Figure 5.135

39. Repeat Problem 38 with $V_A < \infty$.

40. Consider Eq. (5.157) for the gain of a degenerated CE stage. Writing $g_m = I_C/V_T$, we note that g_m and hence the voltage gain vary if I_C changes with the signal level. For the following two cases, determine the relative change in the gain if I_C varies by 10%: (a) $g_m R_E$ is nominally equal to 3; (b) $g_m R_E$ is nominally equal to 7. The more constant gain in the second case translates to greater circuit linearity.

41. Express the voltage gain of the stage depicted in Fig. 5.136 in terms of the collector bias

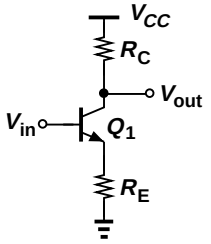


Figure 5.136

current, I_C, and V_T. If $V_A = \infty$, what is the gain if the dc voltage drops across R_C and R_E are equal to $20V_T$ and $5V_T$, respectively?

42. We wish to design the degenerated stage of Fig. 5.137 for a voltage gain of 10 with Q_1 operating at the edge of saturation. Calculate the bias current and the value of R_C if $\beta = 100$, $I_S = 5 \times 10^{-16}$A, and $V_A = \infty$. Calculate the input impedance of the circuit.

43. Repeat Problem 42 for a voltage gain of 100. Explain why no solution exists. What is the maximum gain that can be achieved in this stage?

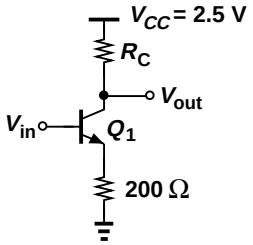


Figure 5.137

44. Construct the small-signal model of the CE stage shown in Fig. 5.43(a) and calculate the voltage gain. Assume $V_A = \infty$.

45. Construct the small-signal model of the CE stage shown in Fig. 5.43(a) and prove that the output impedance is equal to R_C if the Early effect is neglected.

46. Determine the voltage gain and I/O impedances of the circuits shown in Fig. 5.138. Assume $V_A = \infty$.

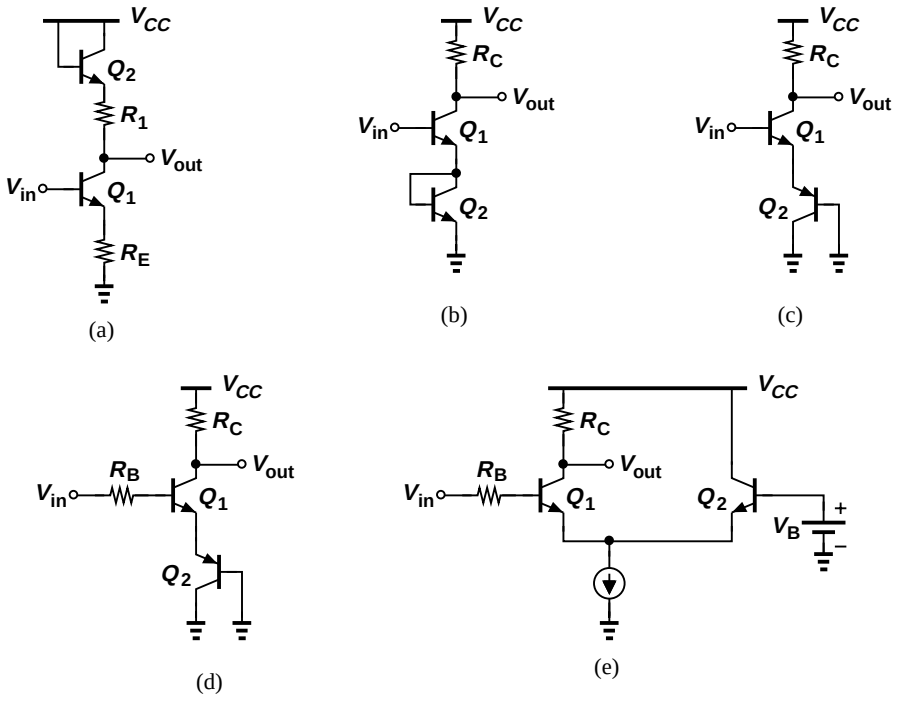


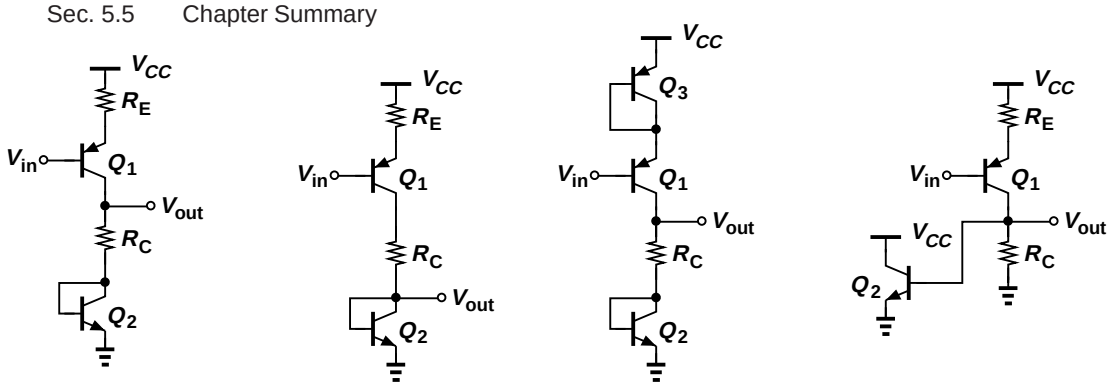
Figure 5.138

47. Compute the voltage gain the I/O impedances of the circuits depicted in Fig. 5.139. Assume $V_A = \infty$.

48. Using a small-signal equivalent circuit, compute the output impedance of a degenerated CE stage with $V_A < \infty$. Assume $\beta \gg 1$.

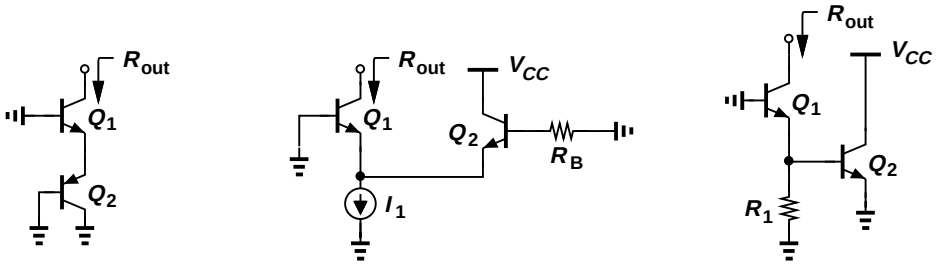
49. Calculate the output impedance of the circuits shown in Fig. 5.140. Assume $\beta \gg 1$.

50. Compare the output impedances of the circuits illustrated in Fig. 5.141. Assume $\beta \gg 1$.



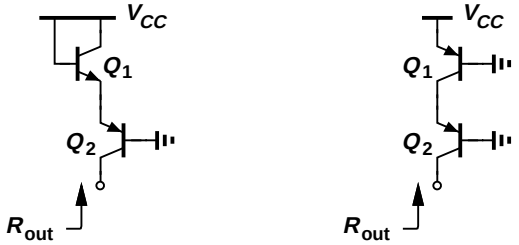
(a) (b) (c) (d)

Figure 5.139



(a) (b) (c)

Figure 5.140



(a) (b)

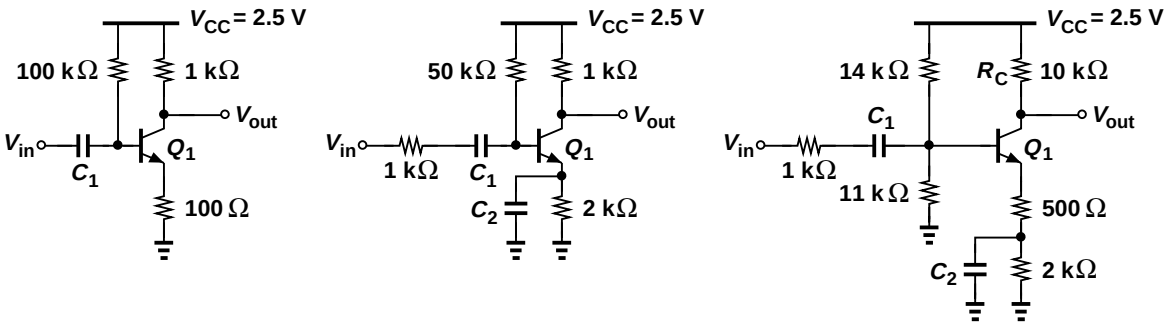
Figure 5.141

51. Writing $r_\pi = \beta V_T / I_C$, expand Eq. (5.217) and prove that the result remains close to r_π if $I_B R_B \gg V_T$ (which is valid because V_{CC} and V_{BE} typically differ by about 0.5 V or higher.)

52. Calculate v_{out}/v_{in} for each of the circuits depicted in Fig. 5.142. Assume $I_S = 8 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$. Also, assume the capacitors are very large.

53. Repeat Example 5.33 with $R_B = 25\text{k}\Omega$ and $R_C = 250\ \Omega$. Is the gain greater than unity?

54. The common-base stage of Fig. 5.143 is biased with a collector current of 2 mA. Assume $V_A = \infty$.
(a) Calculate the voltage gain and I/O impedances of the circuit.



(a) (b) (c)

Figure 5.142

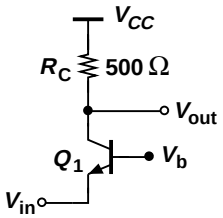
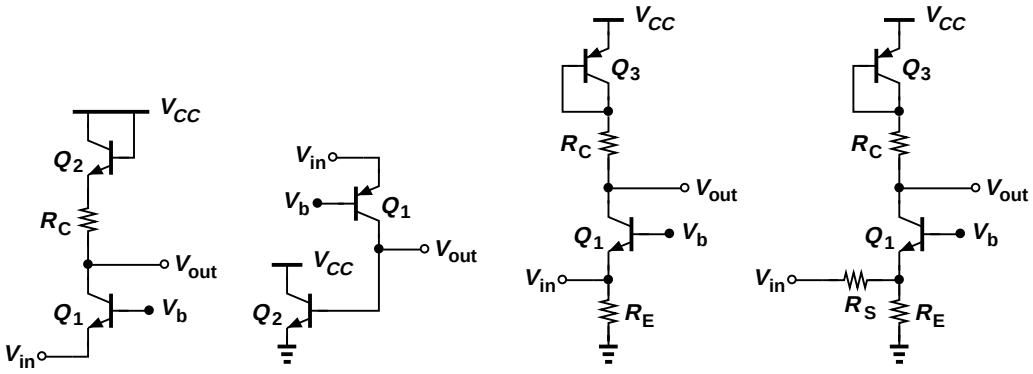


Figure 5.143

(b) How should V_B and R_C be chosen to maximize the voltage gain with a bias current of 2 mA?

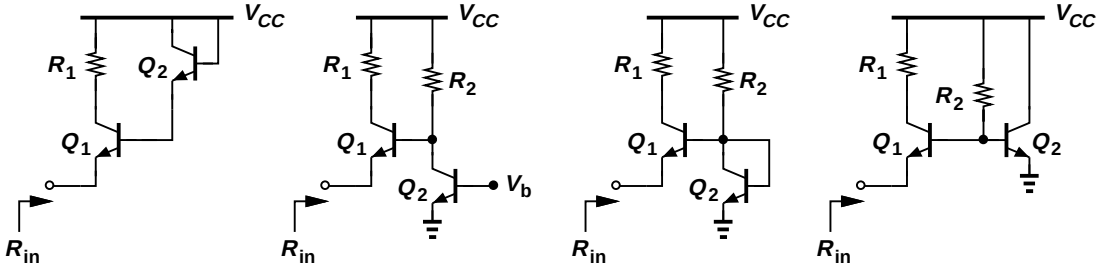
55. Determine the voltage gain of the circuits shown in Fig. 5.144. Assume $V_A = \infty$.



(a) (b) (c) (d)

Figure 5.144

56. Compute the input impedance of the stages depicted in Fig. 5.145. Assume $V_A = \infty$.



(a) (b) (c) (d)

Figure 5.145

57. Calculate the voltage gain and I/O impedances of the CB stage shown in Fig. 5.146. Assume $V_A < \infty$.

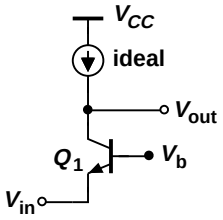


Figure 5.146

58. Consider the CB stage depicted in Fig. 5.147, where $\beta = 100$, $I_S = 8 \times 10^{-16}$ A, $V_A = \infty$, and C_B is very large.

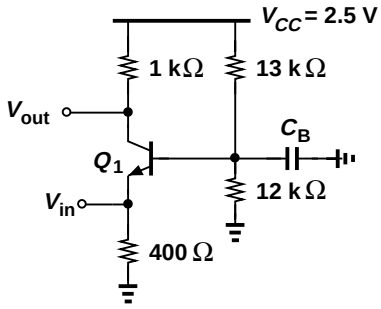


Figure 5.147

(a) Determine the operating point of Q_1.
(b) Calculate the voltage gain and I/O impedances of the circuit.

59. Repeat Problem 58 for $C_B = 0$.

60. Compute the voltage gain and I/O impedances of the stage shown in Fig. 5.148 if $V_A = \infty$ and C_B is very large.

61. Calculate the voltage gain and the I/O impedances of the stage depicted in Fig. 5.149 if $V_A = \infty$ and C_B is very large.

62. Calculate the voltage gain of the circuit shown in Fig. 5.150 if $V_A < \infty$.

63. The circuit of Fig. 5.151 provides two outputs. If $I_{S1} = 2I_{S2}$, determine the relationship between v_{out1}/v_{in} and v_{out2}/v_{in}. Assume $V_A = \infty$.

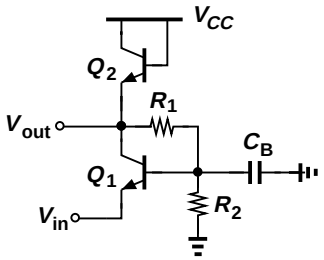


Figure 5.148

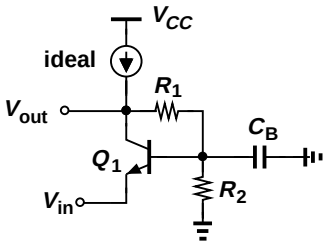


Figure 5.149

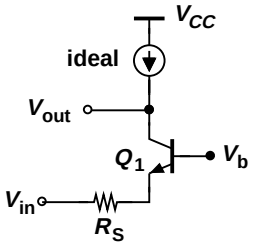


Figure 5.150

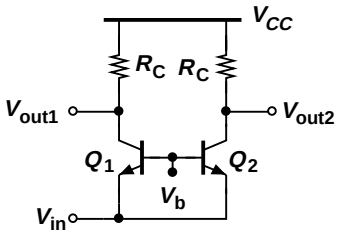


Figure 5.151

64. Using a small-signal model, determine the voltage gain of a CB stage with emitter degeneration, a base resistance, and $V_A < \infty$. Assume $\beta \gg 1$.

65. For $R_E = 100\,\Omega$ in Fig. 5.152, determine the bias current of Q_1 such that the gain is equal to 0.8. Assume $V_A = \infty$.

66. The circuit of Fig. 5.152 must provide an input impedance of greater than 10 kΩ with a minimum gain of 0.9. Calculate the required bias current and R_E. Assume $\beta = 100$ and $V_A = \infty$.

67. A microphone having an output impedance $R_S = 200\,\Omega$ drives an emitter follower as shown

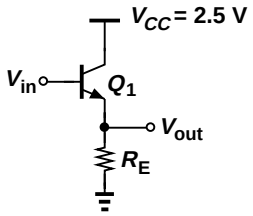


Figure 5.152

in Fig. 5.153. Determine the bias current such that the output impedance does not exceed 5

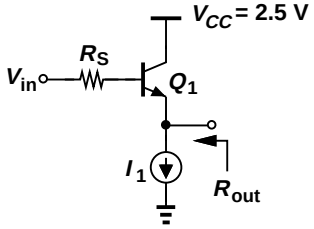


Figure 5.153

Ω. Assume $\beta = 100$ and $V_A = \infty$.

68. Compute the voltage gain and I/O impedances of the circuits shown in Fig. 5.154. Assume $V_A = \infty$.

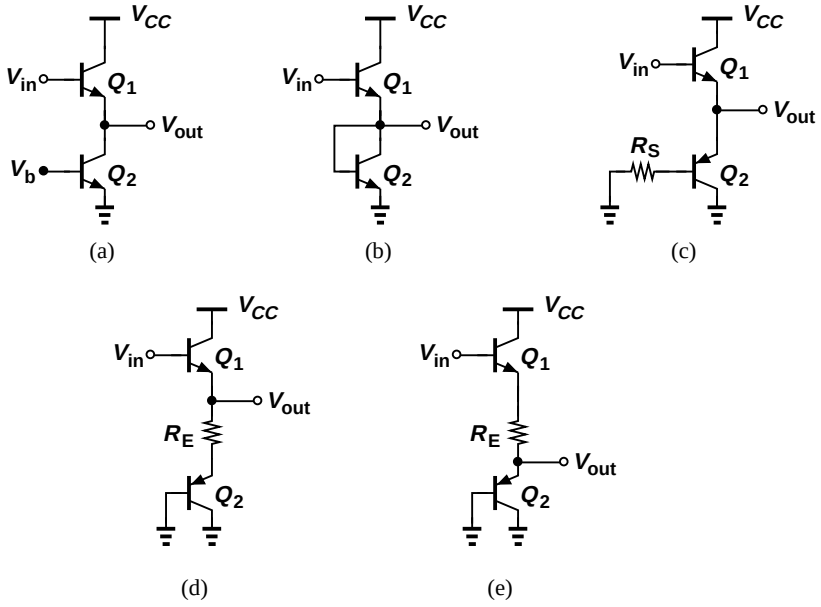


Figure 5.154

69. Figure 5.155 depicts a "Darlington pair," where Q_1 plays a role somewhat similar to an emitter follower driving Q_2. Assume $V_A = \infty$ and the collectors of Q_1 and Q_2 are tied to V_{CC}. Note that $I_{E1}(\approx I_{C1}) = I_{B2} = I_{C2}/\beta$.
(a) If the emitter of Q_2 is grounded, determine the impedance seen at the base of Q_1.
(b) If the base of Q_1 is grounded, calculate the impedance seen at the emitter of Q_2.
(c) Compute the current gain of the pair, defined as $(I_{C1} + I_{C2})/I_{B1}$.

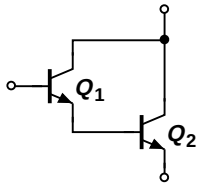


Figure 5.155

70. In the emitter follower shown in Fig. 5.156, Q_2 serves as a current source for the input device

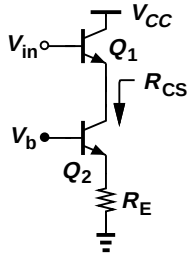


Figure 5.156

Q_1.
(a) Calculate the output impedance of the current source, R_{CS}.
(b) Replace Q_2 and R_E with the impedance obtained in (a) and compute the voltage gain and I/O impedances of the circuit.

71. Determine the voltage gain of the follower depicted in Fig. 5.157. Assume $I_S = 7 \times 10^{-16}$

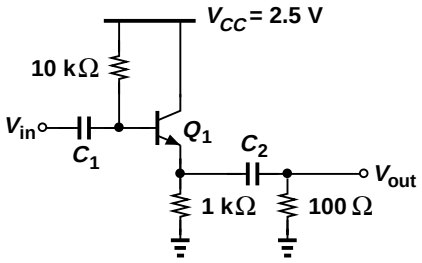


Figure 5.157

A, $\beta = 100$, and $V_A = 5$ V. (But for bias calculations, assume $V_A = \infty$.) Also, assume the capacitors are very large.

72. Figure 5.158 illustrates a cascade of an emitter follower and a common-emitter stage. As-

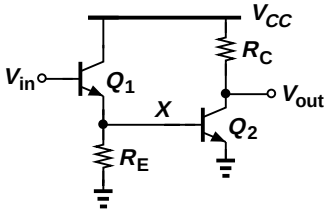


Figure 5.158

sume $V_A < \infty$.

(a) Calculate the input and output impedances of the circuit.
(b) Determine the voltage gain, $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$.

73. Figure 5.159 shows a cascade of an emitter follower and a common-base stage. Assume

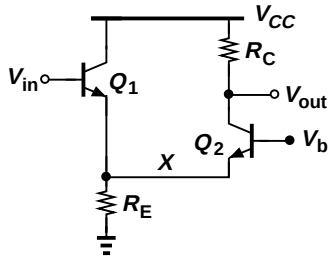


Figure 5.159

$V_A = \infty$.
(a) Calculate the I/O impedances of the circuit.
(b) Calculate the voltage gain, $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$.

Design Problems

In the following problems, unless otherwise stated, assume $\beta = 100$, $I_S = 6 \times 10^{-16}$ A, and $V_A = \infty$.

74. Design the CE stage shown in Fig. 5.160 for a voltage gain of 10, and input impedance of

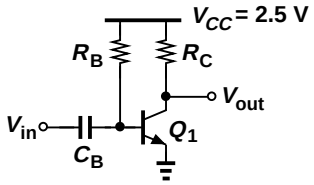


Figure 5.160

greater than 5 kΩ, and an output impedance of 1 kΩ. If the lowest signal frequency of interest is 200 Hz, estimate the minimum allowable value of C_B.

75. We wish to design the CE stage of Fig. 5.161 for maximum voltage gain but with an output

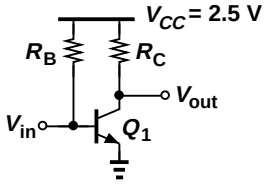


Figure 5.161

impedance no greater than 500 Ω. Allowing the transistor to experience at most 400 mV of base-collector forward bias, design the stage.

76. The stage depicted in Fig. 5.161 must achieve maximum input impedance but with a voltage gain of at least 20 and an output impedance of 1 kΩ. Design the stage.

77. The CE stage of Fig. 5.161 must be designed for minimum supply voltage but with a voltage gain of 15 and an output impedance of 2 kΩ. If the transistor is allowed to sustain a base-collector forward bias of 400 mV, design the stage and calculate the required supply voltage.

78. We wish to design the CE stage of Fig. 5.161 for minimum power dissipation. If the voltage gain must be equal to A_0, determine the trade-off between the power dissipation and the output impedance of the circuit.

79. Design the CE stage of Fig. 5.161 for a power budget of 1 mW and a voltage gain of 20.

80. Design the degenerated CE stage of Fig. 5.162 for a voltage gain of 5 and an output

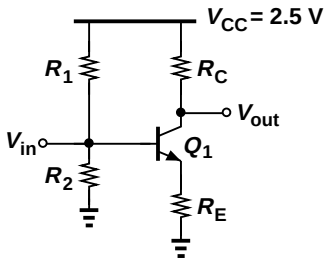


Figure 5.162

impedance of 500 Ω. Assume R_E sustains a voltage drop of 300 mV and the current flowing through R_1 is approximately 10 times the base current.

81. The stage of Fig. 5.162 must be designed for maximum voltage gain but an output impedance of no greater than 1 kΩ. Design the circuit, assuming that R_E sustains 200 mV, and the current flowing through R_1 is approximately 10 times the base current, and Q_1 experiences a maximum base-collector forward bias of 400 mV.

82. Design the stage of Fig. 5.162 for a power budget of 5 mW, a voltage gain of 5, and a voltage drop of 200 mV across R_E. Assume the current flowing through R_1 is approximately 10 times the base current.

83. Design the common-base stage shown in Fig. 5.163 for a voltage gain of 20 and an input

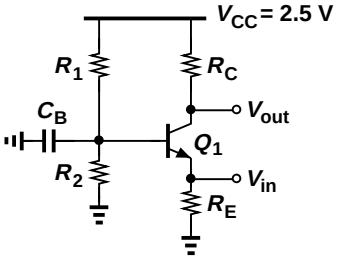


Figure 5.163

impedance of 50 Ω. Assume a voltage drop of $10V_T = 260$ mV across R_E so that this resistor does not affect the input impedance significantly. Also, assume the current flowing through R_1 is approximately 10 times the base current, and the lowest frequency of interest is 200 Hz.

84. The CB amplifier of Fig. 5.163 must achieve a voltage gain of 8 with an output impedance of 500 Ω. Design the circuit with the same assumptions as those in Problem 83.

85. We wish to design the CB stage of Fig. 5.163 for an output impedance of 200 Ω and a voltage gain of 20. What is the minimum required power dissipation? Make the the same assumptions as those in Problem 83.

86. Design the CB amplifier of Fig. 5.163 for a power budget of 5 mW and a voltage gain of 10. Make the same assumptions as those in Problem 83.

87. Design the CB stage of Fig. 5.163 for the minimum supply voltage if an input impedance of 50 Ω and a voltage gain of 20 are required. Make the same assumptions as those in Problem 83.

88. Design the emitter follower shown in Fig. 5.164 for a voltage gain of 0.85 and an input

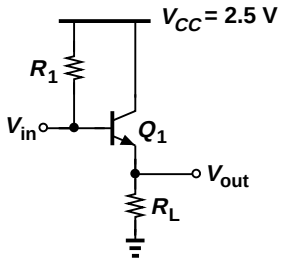


Figure 5.164

impedance of greater than 10 kΩ. Assume $R_L = 200\ \Omega$.

89. The follower of Fig. 5.164 must consume 5 mW of power while achieving a voltage gain of 0.9. What is the minimum load resistance, R_L, that it can drive?

90. The follower shown in Fig. 5.165 must drive a load resistance, $R_L = 50\ \Omega$, with a voltage

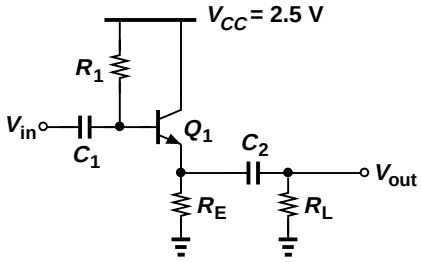


Figure 5.165

gain of 0.8. Design the circuit assuming that the lowest frequency of interest is 100 MHz. (Hint: select the voltage drop across R_E to be much greater than V_T so that this resistor does not affect the voltage gain significantly.)

SPICE Problems

In the following problems, assume $I_{S,npn} = 5 \times 10^{-16}$ A, $\beta_{npn} = 100$, $V_{A,npn} = 5$ V, $I_{S,pnp} = 8 \times 10^{-16}$ A, $\beta_{pnp} = 50$, $V_{A,pnp} = 3.5$ V.

91. The common-emitter shown in Fig. 5.166 must amplify signals in the range of 1 MHz to 100 MHz.

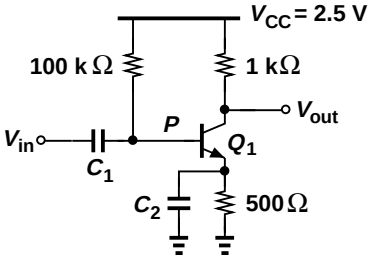


Figure 5.166

(a) Using the .op command, determine the bias conditions of Q_1 and verify that it operates in the active region.
(b) Running an ac analysis, choose the value of C_1 such that $|V_P/V_{in}| \approx 0.99$ at 1 MHz. This ensures that C_1 acts as a short circuit at all frequencies of interest.
(c) Plot $|V_{out}/V_{in}|$ as a function of frequency for several values of C_2, e.g., 1 μF, 1 nF, and 1 pF. Determine the value of C_2 such that the gain of the circuit at 10 MHz is only 2% below its maximum (i.e., for $C_2 = 1$ μF).
(d) With the proper value of C_2 found in (c), determine the input impedance of the circuit at 10 MHz. (One approach is to insert a resistor in series with V_{in} and adjust its value until V_P/V_{in} or V_{out}/V_{in} drops by a factor of two.)

92. Predicting an output impedance of about 1 kΩ for the stage shown in Fig. 5.166, a student constructs the circuit depicted in Fig. 5.167, where V_X represents an ac source with zero dc value. Unfortunately, V_N/V_X is far from 0.5. Explain why.

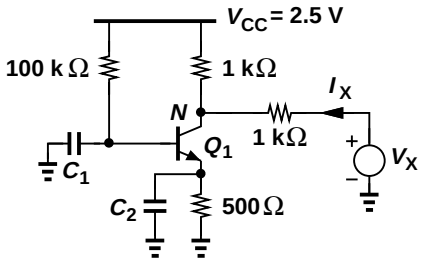


Figure 5.167

93. Consider the self biased stage shown in Fig. 5.168.

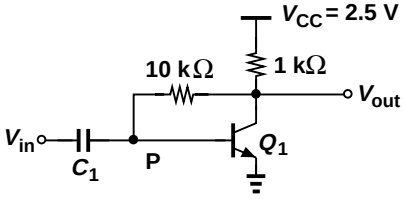


Figure 5.168

(a) Determine the bias conditions of Q_1.
(b) Select the value of C_1 such that it operates as nearly a short circuit (e.g., $|V_P/V_{in}| \approx 0.99$) at 10 MHz.
(c) Compute the voltage gain of the circuit at 10 MHz.
(d) Determine the input impedance of the circuit at 10 MHz.
(e) Suppose the supply voltage is provided by an aging battery. How much can V_{CC} fall while the gain of the circuit degrades by only 5%?

94. Repeat Problem 93 for the stage illustrated in Fig. 5.169. Which one of the two circuits is less sensitive to supply variations?

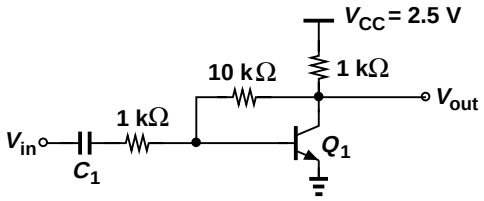


Figure 5.169

95. The amplifier shown in Fig. 5.170 employs an emitter follower to drive a 50-Ω load at a frequency of 100 MHz.

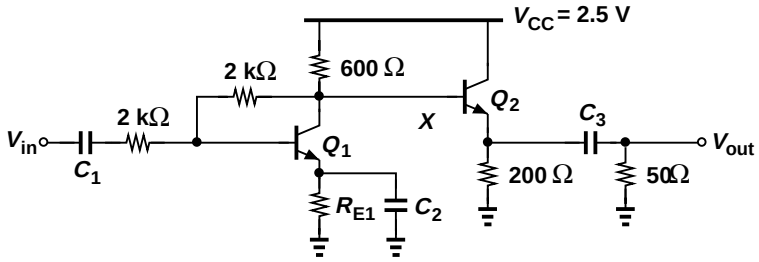


Figure 5.170

(a) Determine the value of R_{E1} such that Q_2 carries a bias current of 2 mA.
(b) Determine the minimum acceptable value of C_1, C_2, and C_3 if each one is to degrade the gain by less than 1%.
(c) What is the signal attenuation of the emitter follower? Does the overall gain increase if R_{G2} is reduced to 100 Ω? Why?