# Frequency Multipliers

Iulian Rosu, YO3DAC / VA3IUL, http://www.qsl.net/va3iul

There are few approaches how to generate a high frequency signal for microwaves frequencies.

Direct Signal Generation -

First approach is to generate the high frequency directly, at the fundamental, using an oscillator tuned on the desired frequency. Few sensitive issues appears here due to high working frequency as, stability, jitter, phase noise, pulling, pushing, low output power, and cost of the active component to meet the performances.

A FET oscillator may be stabilized by a dielectric resonator. Problems may involve in this situation are: phase noise, frequency stability and accuracy.
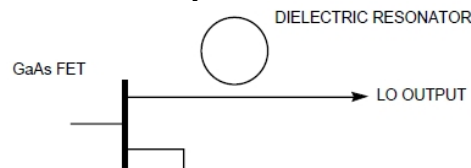
Sub-Harmonic Mixer -

Another approach how to minimize the issues of a high frequency oscillator is to use a Sub-Harmonic mixer.
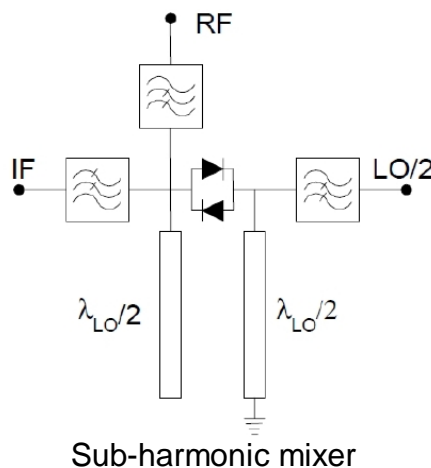

Sub-harmonic mixer

- Sub-harmonic mixers are useful at higher frequencies when it can be difficult to produce a suitable LO signal. They have the LO input at frequency = LO/n.
- Sub-harmonic mixers use anti-parallel diode pairs and they produce most of their power at *"odd"* products of the input signals. Even products are rejected due to the I-V characteristics of the diodes.
- Attenuation of even harmonics is determined by diodes "balance". The diode "matching" is critical in this type of mixers.
- The short circuit $\lambda_{LO}/2$ stub at the LO port is a quarter of a wavelength long at the input frequency of LO/2 and so is open circuit. However, at RF frequency this stub is approximately a half wavelength long, so providing a short circuit to the RF signal.
- At the RF input the open circuit $\lambda_{LO}/2$ stub presents a good open circuit to the RF but is a quarter wavelength long at the frequency LO/2 and so is short circuit.

Up-Conversion Mixer -

The third option to generate a high frequency signal is to use an up converter. The design of an up converter has typically received much less attention in terms of design methodology than down converter design, which is common approach in most of the receiver designs. There are some aspects to up converter design which are not relevant to down converters, and vice versa.

- An up-conversion mixer requires high linearity and low noise to minimize the amount of spurious power spread into adjacent channels.
  Have to take careful attention at LO amplitude, and LO-to-RF isolation.
- A good approach for an up-conversion mixer is the balanced mixer which provides good common-mode rejection to suppress LO feed-through and good linearity.
- The LO level should provide a reasonable compromise between conversion gain and LO power, but should not limit the 1 dB gain-compression input voltage.
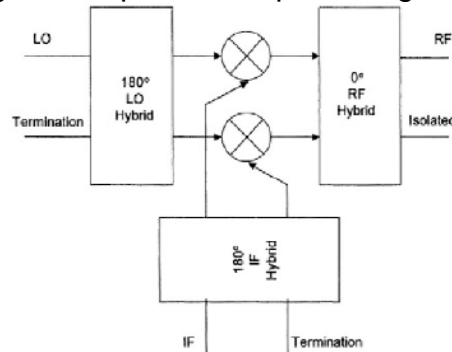

Balanced up-conversion mixer
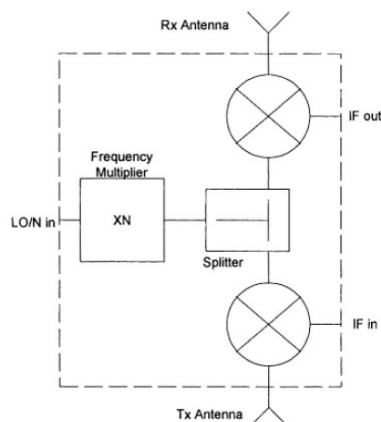
Frequency Multipliers –

Another alternative method to generate high frequency signal power with low phase noise is to generate a high-quality lower frequency signal and employ a frequency multiplier to deliver the high frequency output at the desired frequency. This approach is the subject of this paper.

Frequency multipliers will always be a way of generating the highest frequencies.

- A frequency multiplier has the property that the frequency of the output signal has an integer multiple of the input frequency.
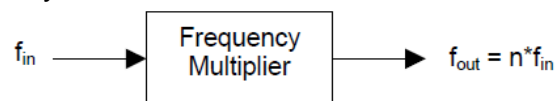
This approach is commonly adopted in microwave transceivers.

Frequency multiplier based microwave transceiver block diagram

Even if a multiplier introduces no Phase Noise of its own, the process of frequency multiplication even by an ideal, noiseless multiplier, inevitably increases the Phase Noise.

- The reason for this unfortunate characteristic is that a frequency multiplier is in fact a phase multiplier, so it multiplies the phase deviations as well as the frequency of the input signal.
- A square-wave contains odd harmonics. However, by varying the duty cycle of the waveform, so that rectangular-wave results, even order harmonic content can be introduced.
- The 2nd harmonic content of a rectangular-wave peaks when the duty cycle is *25%*, and a 3rd harmonic peaks when duty cycle peaks 16%.
- The minimum Carrier-to-Noise degradation, *ΔCNR*, in decibels, caused by an ideal frequency multiplier is:

$$\Delta CNR_{[dB]} = 20*LOG\ (N) \quad \text{where N is the multiplication factor.}$$

- Thus, a frequency doubler (N=2) degrades CNR at the input signal by at least 6dB and a quadrupler (N=4) degrades CNR by at least 12dB.

Multiplying a very stable low-frequency reference signal can still produce signals with better Phase Noise than producing them directly in the microwave frequency range.

- For example typical Phase Noise of a 10 MHz Crystal Oscillator is: -170 dBc/Hz @ 100 kHz offset.
- Using a multiplier chain (10 x 24 = 240) to get a 2.4 GHz signal, degrades this Phase Noise by 20*LOG(240) = 48 dB, yielding: -170 dBc/Hz + 48 dB = -122 dBc/Hz @ 100 kHz offset.
- Compare this Phase Noise to a standard LC-tank oscillator working directly at 2.4 GHz, which has a typical Phase Noise of -100dBc/Hz @ 100 kHz offset.

A frequency multiplier circuit should contain a nonlinear device and filters that enable to select the desired component at the output and separate the source from the generated harmonics.

Frequency Multiplier Chain with Filters
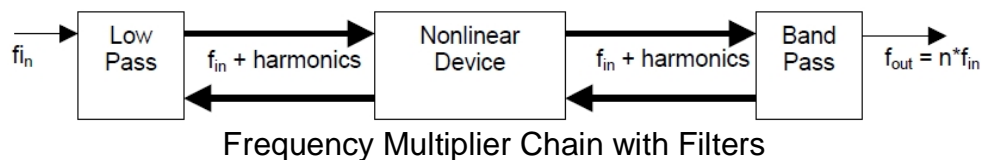
- The nonlinear device will produce voltages of higher order from the current of the first harmonic. One of these voltages is of the desired order and will be allowed to exit through the band-pass filter.
  Low-pass and band-pass filters will present high impedance to all unwanted harmonic voltages.
- But it turns out that if we allow the currents of the other harmonics to flow, the intermodulation products of those harmonics will contribute to the desired harmonic of the output frequency. That means we should try to short the currents of the non-desired harmonics.
- As we want to deliver as much power as possible to the load the frequency multiplier should be matched at the input (for the input frequency) and at the output (for the output frequency).

To obtain higher order frequency multiplication we can cascade several multipliers. This can increase conversion efficiency but also increases complexity.

There are different possibilities concerning the nonlinear device:
- We need a device with a nonlinear characteristic in order to produce higher order harmonics.
- The nonlinear characteristic might be a nonlinear I-V or C-V relationship.
- Usually wideband multipliers use a nonlinear I-V characteristic, but when we want to design a frequency multiplier with high efficiency, and not high bandwidth, we prefer the nonlinear C-V characteristic. For example a varactor diode has a nonlinear C-V characteristic.

Frequency Multipliers Waveforms

Any non-sinewave repetitive waveform contains energy at harmonics of the fundamental frequency.

The task is to create a non-linear circuit that produces a waveform with significant signal strength at the desired harmonics.

Figure below shows the amplitude terms (peak value of the nth harmonic sine wave) for various waveforms.
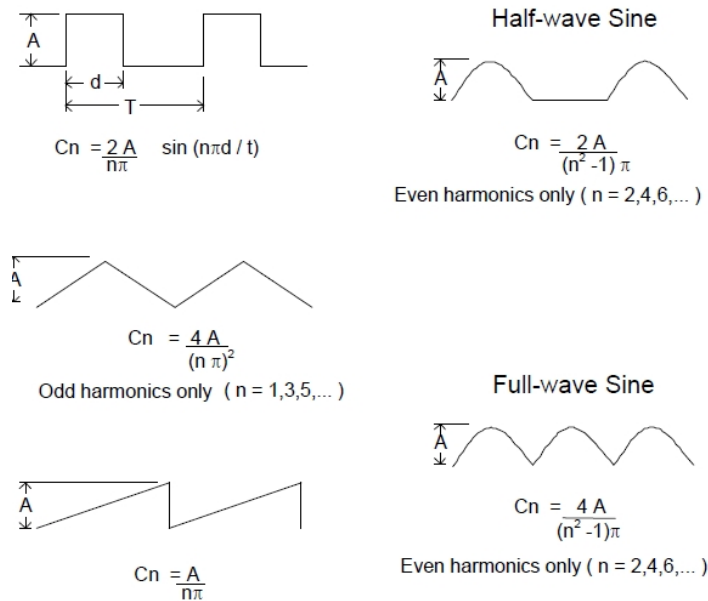
Harmonic amplitude terms for various waveforms (C. Wenzel)

- Can be seen that waveforms with fast edges have larger high frequency harmonics.
- Harmonics without vertical edges have n^2 in the denominator, but the waveforms with fast edges only have n in the denominator.
- The timing (duty-cycle) between the positive and negative edges of a pulse determines which harmonics are emphasized. For example, a 50% duty-cycle square-wave has only odd harmonics. In this situation the timing is wrong for the buildup of even-harmonic energy, but a 25% duty-cycle contains large even harmonics: the edges occur at the right time to reinforce certain even harmonics.

Figure below shows the harmonic content of a square pulse as a function of its duty-cycle.
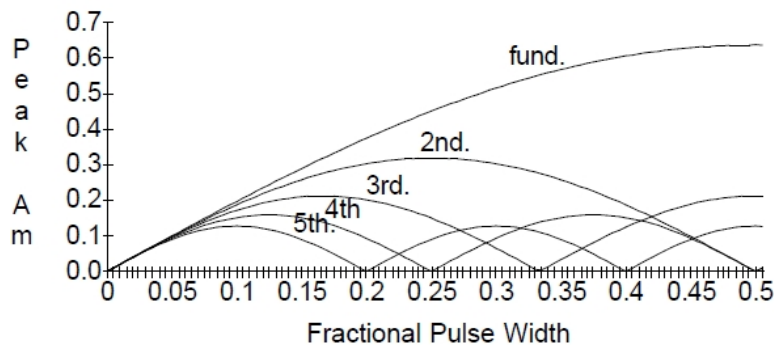
Square Pulse Harmonic content vs Duty-Cycle (C. Wenzel)

As was mentioned before the chart suggests that the most 2nd harmonic energy will be generated when the duty-cycle is 25%. But it can also be seen that if the duty-cycle is increased to 33% then the third harmonic drops to zero which could simplify output filtering with little drop in the desired 2nd harmonic.

Frequency Multipliers Characteristics

- **Conversion Loss and Maximum Input Signal Power**

Semiconductor diodes used in microwave frequency multipliers are essentially lossy passive devices and for this reason they dissipate energy. Embedding circuits also dissipate energy. As a result, multiplier's input/output power conversion efficiency is less than unity.

Conversion Loss used to characterize microwave frequency multiplier's conversion efficiency is defined as the ratio of the available source power Pin_{source} to the output harmonic power $Pout_{harmonic}$ delivered to the load.

Conversion Efficiency is defined as the ratio of the output power Pout delivered to the load to the available power of the input source Pin, and usually is expressed in percent.

The goal of the circuit design is to minimize the conversion loss (or maximize the conversion efficiency) for a given device and input/output frequencies.

When get low conversion efficiency, virtually all the input power is dissipated in the nonlinear element. The maximum input power is limited by the device power handling capability and must be clearly stated when specifying a frequency multiplier.

- **Source and Load Impedance**

 One of the conditions for a diode frequency multiplier to achieve minimum conversion loss is that optimum source and load impedances should be provided to the diode.

The source impedance should be very close to the complex conjugate of the multiplier input impedance Zin to minimize reflection loss at the input.

The load impedance should be equal to the optimum load value, otherwise leads to an increased conversion loss or decreased output power.

- **Bandwidth**

BW represents the output or input frequency range over which conversion loss is in the specified limits.

- **Harmonics**

A nonlinear device produce undesired harmonics along with the desired ones, and this might affect the performance of the system where the multiplier is used.

- **Noise Conversion**

In all practical situations the resulting noise sidebands are subject of frequency conversion together with the carrier. The multiplier devices add their own noise, and is important to predict the resulting output noise spectrum.

- **Phase Noise Conversion**

All frequency multipliers will increase the phase noise by the same factor (N) that they multiply, because frequency and phase are both multiplied. In dB this would be 20 log N.

Diode Frequency Multipliers

Diode frequency multipliers can be generally classified as being of varistor (Schottky barrier diode) or varactor type.

In the first case, frequency multiplication is performed by a nonlinear resistance or conductance with consequent poor conversion efficiency but a very large potential bandwidth.

In the varactor case a nonlinear reactive element (with nonlinear capacitance) is used.

Varactor type multipliers have high potential conversion efficiency, but exhibit a narrow bandwidth and a high sensitivity to operating conditions, and sometimes stability problems.

In theory, a cascade of low-order multipliers usually has greater efficiency than a single high-order multiplier, but must consider the additional losses in cascading two multipliers (it is invariably necessary to use an isolator between them), and especially the additional cost.

Resistive (Varistor) Frequency Multipliers

- Resistive frequency multipliers use the nonlinear I-V characteristic of a Schottky-barrier diode to distort a sinusoidal waveform. This distortion generates harmonics.
- The more is distorting the input sinusoid, the greater the harmonic currents in the diode, but the maximum still not very great because resistive frequency multipliers are not very efficient.
- In theory a diode doublers have 6dB conversion loss ($1/N^2$) but in reality the conversion loss is about 10dB and there is no reason to make higher-harmonic resistive multipliers.
- The advantage of resistive multipliers is, they are very broadband.
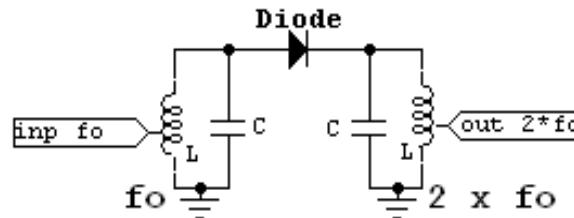
Simplified model of a Resistive (diode) Frequency Doubler

The parallel LC resonators are ideal because they short-circuit the diode at the unwanted harmonics, decoupling the input from the output, and put the diode in parallel with the input at the fundamental frequency and in parallel with the output at the second harmonic.
The inductor can be tapped to optimize the source and load impedances of the diode.

The frequency doubler using microstrip lines presented below is suitable for microwave frequencies.
- The circuit use a λ/4 at fo, short-circuited through a stub at the input side of the Schottky diode (which is equivalent to λ/2 at 2xfo), which is used to create a short-circuit at 2xfo to prevent the output power generated in the diode from traveling backward.
- Similarly use a λ/4 at fo open-ended stub at the output side, which creates an RF short at fo and causes the input signal penetrating through the diode to be reflected back to the diode.
- A section of the transmission line is used as an inductor to resonate the diode junction capacitance.
- The λ/4 impedance transformers at the input and output are used to transform 50 ohms source and load to optimum diode impedance terminations.
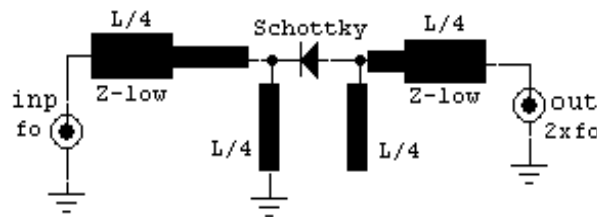
Microwave Microstrip Frequency Doubler

Varactor Diode Frequency Multipliers

A nonlinear reactance also can distort the sinusoidal signal.
- The pros and cons of varactor multiplier are the opposite of those of resistive multiplier.
- A varactor is capable of higher efficiency and higher power than a resistive multiplier, theoretically 100% for all harmonics, but they are very narrowband.
- A design issue of varactor multipliers is they are extreme sensitive to almost every parameter of the circuit, and small changes in the circuit parameters (tuning reactances, bias voltages, input power level, etc) change the output power.
- Making a varactor multiplier work (and keep working) needs a lot of empirical tuning.
- Varactor diode frequency multipliers in general generate very little noise (phase- as well as amplitude noise). The only noise source is the thermal noise of the series resistance of the varactor and the circuit loss resistances.

- The power capability of a varactor multiplier is limited by the device's break-down.
- The varactor always has a parasitic resistance in series, which dissipates power.

In order to minimize the loss power, one would tend to present an open for all the undesired harmonics, resulting in zero current and therefore no loss.

At the example of the pure square-law diode we see that it produces only a 2nd order harmonic directly. This is the reason to present a short to the undesired (intermediate) harmonics.

- The shorting circuits are called idlers.
- Without idlers the varactor multiplier does not generate harmonics efficiently beyond the 2nd harmonic.
- If a current at the 2nd harmonic is prohibited, we don't get the desired higher order harmonics.
- If current is allowed at the 2nd harmonic, it will mix with the first harmonic and generate therefore higher order harmonics.
- A varactor tripler (x3) can be obtained only with a second harmonic idler.
- A varactor quadrupler (x4) could have a 2nd harmonic idler, or both a 2nd harmonic and a 3rd harmonic idler.
- A varactor quintupler (x5) would likely have at least 2nd and 3rd harmonic idlers.

Idlers are usually realized as short-circuit resonators that are separate from the input and output matching circuits.

In practice, idlers are usually realized by a series resonance that is chosen more for its convenience than for high performance.

- Frequently, the series resonance of the varactor's package is used as an idler at high frequencies, and tuning elements are often included to tune the resonance precisely to the desired harmonic.
- To minimize power dissipation and thus to obtain high efficiency, is essential to use high unloaded Q (low-loss) idler resonators.
- Both phase noise and amplitude noise are strongly dependent on the level of the input signal pumping the diode.
- Varactor frequency multipliers are relative unstable. Their instability is a kind of chaotic process, not a simple oscillation.

Controlling the broadband embedding impedance characteristic very carefully is the best way to insure good stability. In particular, the input source and output load must be linear and not vary with input or output level. One must not drive a mixer's LO port directly from a multiplier, or the multiplier directly from another multiplier; an isolator should be used. The input and output networks must not have any spurious resonances.

Introducing a resistor in the diode's DC return path, this current can be used to bias the diode. The resistor also helps to reduce the sensitivity of the output power level to the input power level; as input drive is increased, the resulting increase in DC current further reverse-biases the diode, reducing the multiplier's efficiency and leveling the output power. The design of the bias circuit often has a strong effect on stability. Low frequency resonances in the bias circuit are a common cause of instability.

Lumped elements Frequency Tripler   Distributed Elements Frequency Doubler
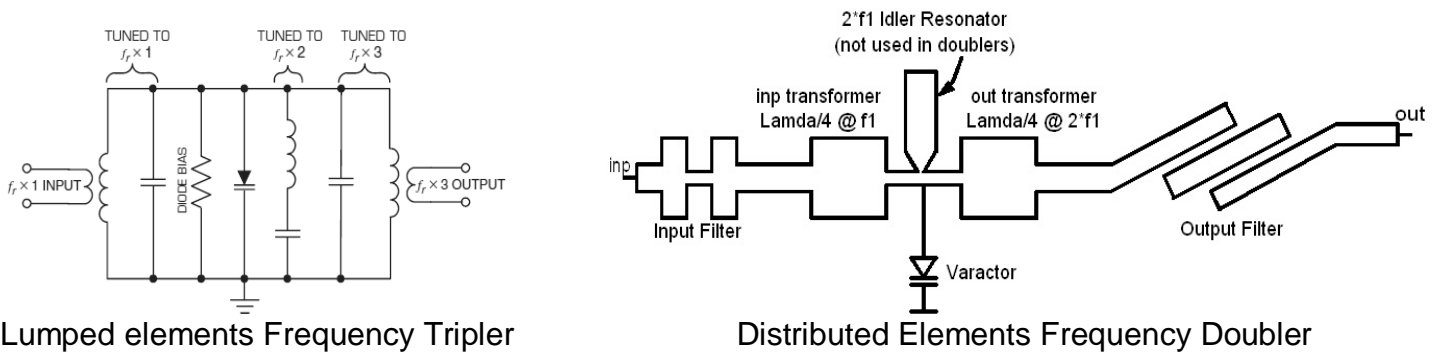
A variant of varactors are Schottky-Barrier varactor diodes which can obtain output frequencies of up to several hundred of GHz.

- One of the most important advantages of Schottky-Barrier based multipliers is the generation of odd harmonics without filtering the even ones.
- This capability is based on the symmetry of the electrical characteristics for unbiased devices. Thus, the load impedances for even harmonics have no effect on the efficiency characteristic.

Step Recovery Diode and PIN Diode Frequency Multipliers

Step Recovery Diodes (also called snap-off diodes) are based on a PIN configuration.
They are commonly employed in the design of frequency multipliers of high order.
Step Recovery Diodes have relatively little capacitance change under reverse bias and are used for higher efficiency applications.
A conventional step recovery diode multiplier consists of a diode, a biasing resistor, and matching filters at input and output. The output filter reflects the un-tuned harmonics back to the diode where they mix to form additional power at the tuned frequency.
- Step Recovery Diodes do not require idler circuits to enhance efficiency (as varactors).
- The SRD multiplier is a reactive multiplier and theoretically doesn't have the efficiency limitation $(1/N^2)$ as resistive multipliers.
- In the design of high-order frequency multipliers, the efficiency of Step Recovery Diodes is much higher than that of varactor diodes. There is, however, a limit to the output frequency of the multiplier circuit.

Single Diode multiplier is useful mainly for low-cost, low-performance applications or high frequency waveguide structures where fundamental frequency is easy to reject. A single diode multiplier has the advantage of easy to provide DC bias to it, which will help optimizing the multiplier.
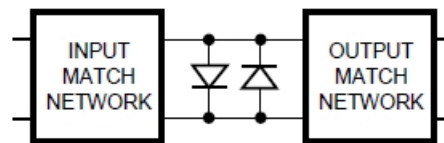A conventional diode multiplier can use one diode or an anti-parallel pair of diodes.
The additional diode results in the suppression of even order products, the enhancement of odd order products, and the elimination of the bias resistor.
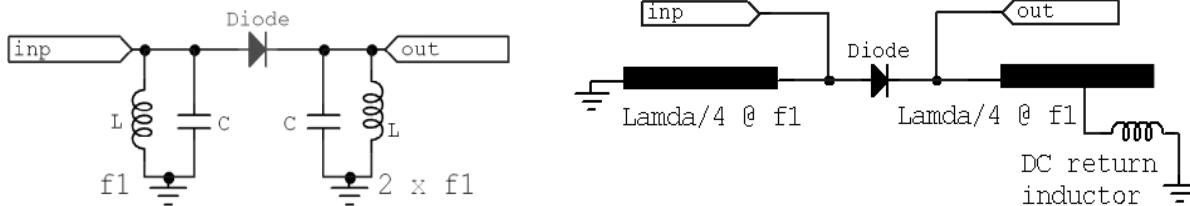
Single diode multipliers – lumped and distributed elements
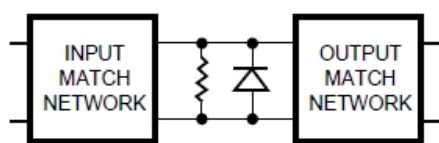

Single Diode Multiplier   Anti-Parallel pair of Diodes

Balanced Diode Multipliers have significant advantages compared to single-ended multipliers; the most important are increased output power and inherent rejection of the fundamental frequency and of certain unwanted harmonics.
The input or load impedance of a balanced multiplier in some cases differs by a factor of two from that of a single-diode multiplier; therefore, a balanced multiplier sometimes provides more satisfactory input or load impedance.
The antiparallel diode connection is probably the simplest form of a balanced multiplier; it rejects even harmonics of the input frequency and consequently can be used only as an odd-order multiplier.
In an antiparallel-diode multiplier, each diode effectively short circuits the other at the second harmonic, so each diode acts as a type of idler for the other. This circuit does not reject the fundamental frequency, however, so it requires an output filter.

x5 Frequency Multiplier using anti-parallel PIN diodes
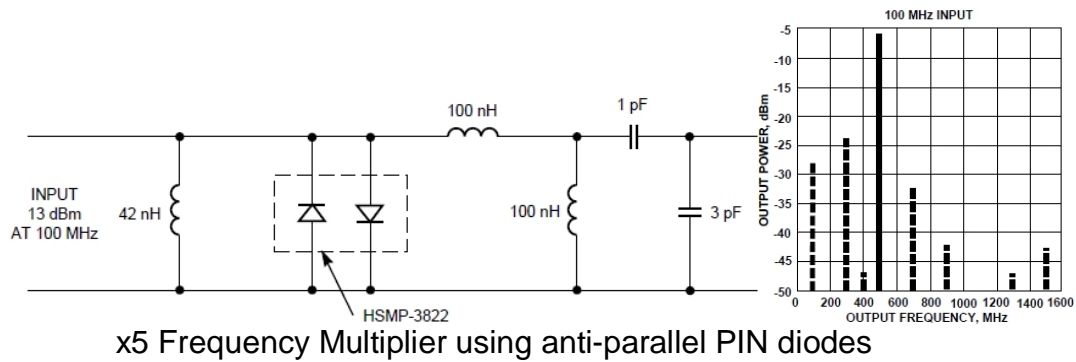
The above circuit is an x5 multiplier operating from a 100 MHz input at +13 dBm, and frequency output at 500MHz and level at about -6dBm. The input was matched with a shunt inductor, and other passive components were added to the output to provide filtering of unwanted signals.

Because the stability of a varactor multiplier is sensitive to small unbalance between the diodes, varactor multipliers are rarely realized as anti-parallel circuits.

Frequency Tripler using Step Recovery Diodes
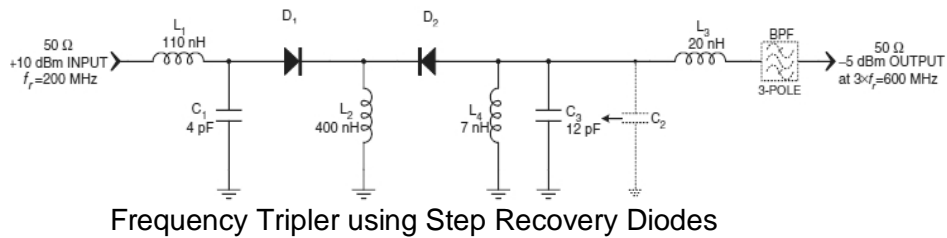
The circuit below shows a singly balanced multiplier using a balun transformer. The difference compared to a DC power supply circuit (which looks like) is, that in a power supply we are looking only for DC component, filtering all the harmonics, when here we are looking for 2nd harmonic, shorting the DC current using an RF choke.
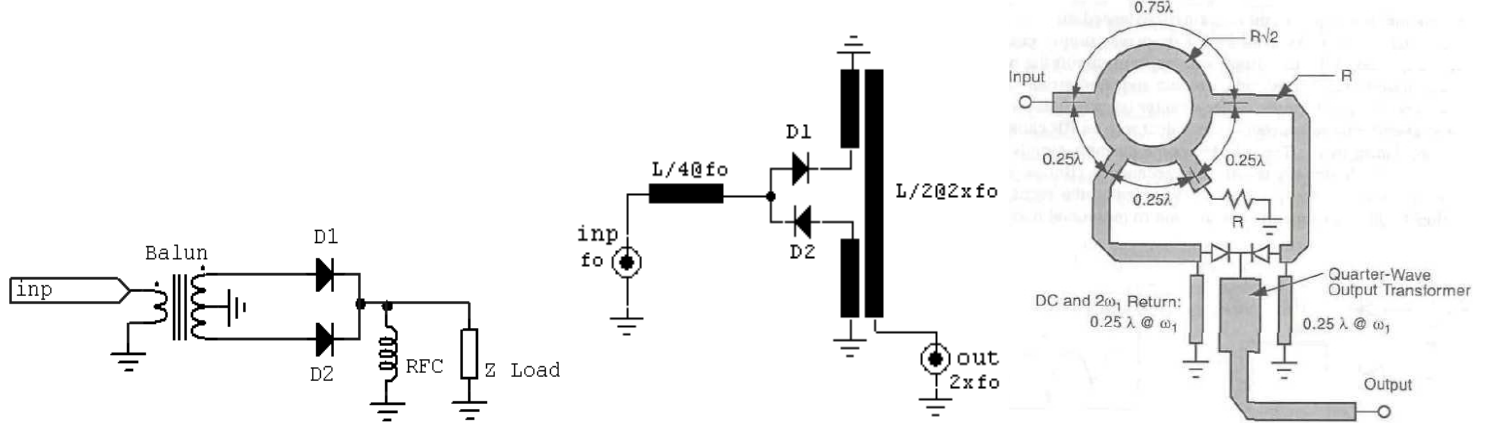

Singly Balanced frequency doublers using: Transformer balun, Microstrip balun and Rat-Race Hybrid

The **Bridge Rectifier** circuit is a practical way to realize resistive frequency doublers.

The design of these multipliers is not the same as the design of a diode ring mixer because the diodes are connected as in a different manner. The ring mixers require baluns when the bridge rectifier requires transformers.

The voltage and current waveforms in the balanced bridge multiplier are identical to those of a full-wave rectifier in a DC power supply. The current consists of a train of half-sinusoidal pulses, which has no odd harmonic components.

Thus, the multiplier inherently rejects the two most troublesome harmonics, the first and third, and the fourth is usually weak enough to require little or no filtering.
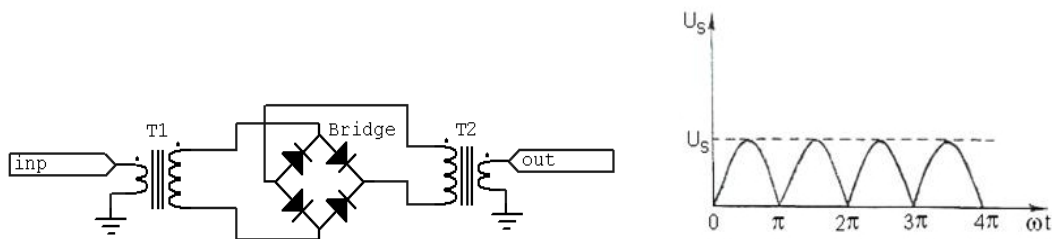
Bridge Diode Frequency Doubler

Charles Wenzel got an RF Design Award for the bridge frequency tripler presented below.
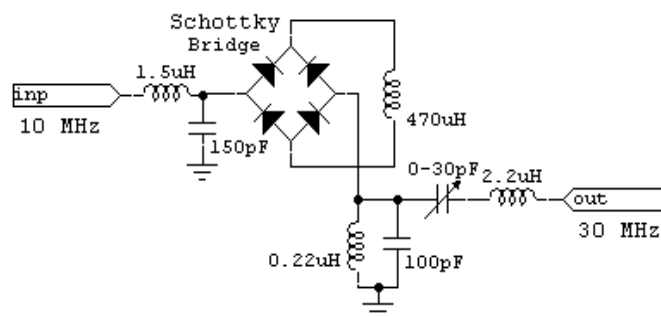
Wenzel Bridge Diode Frequency Tripler

How the circuit works:
- The heart of the multiplier is a sinewave to squarewave converter circuit, which basically is simply a full-wave bridge diode (Schottky barrier) with an inductor short-circuiting the DC terminals.
- The inductor is chosen to have high impedance at the operating frequency so that an AC input results in DC in the inductor.
- This DC flows through alternate pairs of diodes due to the commuting action of the input voltage.
- Therefore, if one AC terminal of the bridge is driven with low impedance sinewave, the other AC terminal will supply a squarewave to a low impedance load.
- The load must have low impedance since the compliance of this current source is exactly equal to the input voltage.
- Because the diodes switch at the input signal's zero crossing the circuit introduce a minimum of AM/PM conversion.
- The input matching network it provides a low impedance to ground for the switching current; and it isolates the input from the switching current.
- The output network presents the required low impedance to the bridge while directing the desired harmonic to the output.
- The conversion efficiency is as high as diode frequency doublers, even though the multiplication factor is higher.
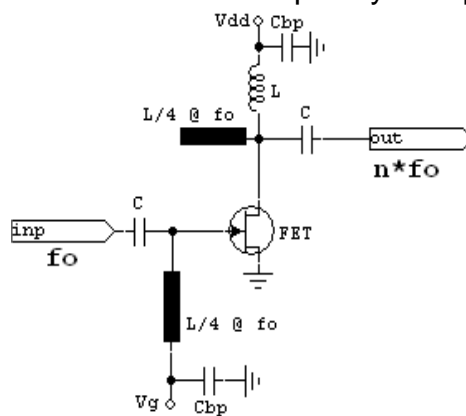
Active Frequency Multipliers

The main reason using active frequency multipliers is they got better efficiency compared to diode frequency multipliers, at the expense they have worst noise levels compared to varactor diodes.
In contrast to diode multipliers which always exhibit loss, FETs or BJTs multipliers can achieve conversion gain over broad bandwidth while getting also good DC to RF efficiency.

The same as amplifiers the active frequency multipliers work in different classes.
A practical form for an active frequency multiplier is to operate in equivalent Class-B power class, where they are very stable and have good gain, efficiency, and output power.

- An active FET frequency multiplier generates harmonics by rectifying the sinusoidal input signal when is biased near its turn-on point (pinch-off), and the input sinusoid turns the device on over part of its cycle.
  - The condition is obtained by applying a positive drain voltage and a negative voltage to the gate. A practical application is to replace the negative supply to a self-bias source resistance, and a gate grounding resistor.
  - The duty cycle of the input signal is adjusted to maximize the desired output harmonic.
  - The higher the harmonic, the shorter the duty cycle must be.
  - For a frequency doubler the optimum duty cycle is about 25% (1/4) when for a frequency tripler is about 16% (1/6).

Figure below shows the circuit of a basic broadband frequency multiplier that uses an ideal FET.

Broadband Active Frequency Multiplier (FET)

- The output resonator is tuned to the nth harmonic of the excitation frequency, so it short circuits the FET's drain at other frequencies, especially the excitation frequency (fo) by using an λ/4 open stub.
- The gate-bias voltage Vg in an efficient FET multiplier must be equal to or less than (more negative than) the threshold voltage, Vt. In this case the FET's channel conducts only during the positive half of the excitation cycle, and the drain conducts in pulses; the shape of the pulses is approximately a rectified cosine.
- The duty cycle of the pulses varies with the DC gate bias, Vg.
- If Vg = Vt the duty cycle is 50%,
- If Vg < Vt (the usual situation), the FET is turned off over most of the excitation cycle. The duty cycle in this case is less than 50%.
- If Vg is much smaller than Vt the magnitude of the peak reverse voltage establishes a limit on the difference.

The second important bias point (after Class-B) is with zero gate voltage, which sometimes is referred as Class-A multiplier. This bias point should give the same performance as the pinch-off, if the gate voltage swings from zero to pinch-off and a low-impedance is connected to the drain.

Microwave transistors are unconditionally stable only within certain frequency ranges, usually above a certain minimum frequency, and we know that the load termination at the fundamental frequency has a major effect on circuit stability.

- Because the load termination controls the series and parallel resonance of the transistor parasitics, and is controlling the peak of the rectified current or the distorted drain voltage, it will affect the multiplier gain, input impedance and bandwidth.
- The proper drain termination is the one that induces the highest peak current. This is obtaining by short-circuit at the fundamental frequency. Ideally the load should be short circuit at all harmonic

frequencies, but the presence of a load at a specific harmonic deviates the signal trajectory in the input plane and the load line becomes a function of frequency.
- Sometimes using other terminations, especially an open-circuit drain termination at the fundamental frequency, has advantages over a short circuit. The primary advantage of using other terminations is that greater gain can be achieved, although the increase in gain usually is the result of undesirable feedback and getting unpredictable oscillation.
- To get a good conversion gain the input power should not be very high.
The required input power is proportional to square of fo (fo^2), so the required input power increases 6 dB per octave; or, in other terms, the available gain decreases by 6 dB per octave. If the input is well matched across a broad bandwidth, a gain slope inevitably results.

The generation of harmonics using FET transistors can be done not only from current or voltage clipping, but also due to mixing of fundamental frequency, and any one of the generated harmonics.
One way to use mixing is to reflect all generated harmonics back to the drain and the other is to feed them back to the gate.
- The initial step in an active multiplier design is to find the performances of the active device at fundamental frequency, looking to parameters as: transconductance *gm*, transition frequency *ft*, and the maximum oscillation frequency *fmax*.
- The transconductance (*gm*) has a direct impact in the device's power performance and multiplication gain, and *ft* and *fmax* determined the limits to be used as a frequency multiplier.

Harmonic Load Pull Test

This is a method which employs no device model and is essentially an experimental process. This method is very useful designing a nonlinear frequency multiplier.
- The active device is inserted into a circuit that has the input tuned at the fundamental frequency and the output tuned at the desired harmonic frequency.
- The active device is than removed and the matching networks are measured using a Vector Network Analyzer, getting the desired impedances which to be applied to the device.
- After that, a conventional linear simulator could be used to synthesize the matching network.

Frequency FET Doublers

Below is presented a **High-Frequency Doubler** using a high frequency FET transistor.
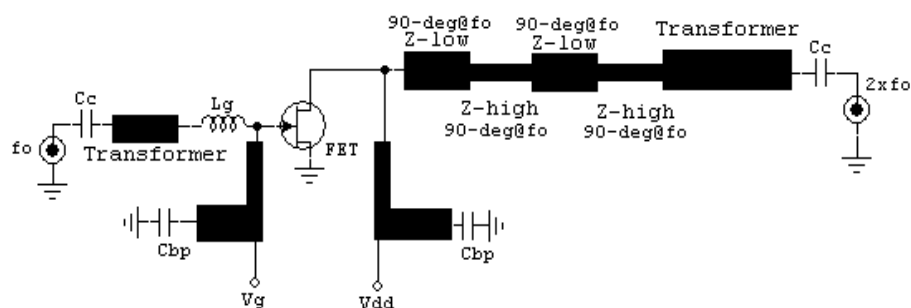

High-Frequency FET Doubler

- To get good input VSWR and maximum power transfer, the input is conjugate matched using microstrip distributed and lumped elements.
- For moderate bandwidth (less than 30% of the center frequency), can resonate the input capacitance with a series inductor. For uniform conversion gain may need to match the input best at highest frequency of the band.
- The output matching network it consists of a filter, to short-circuit the drain at the fundamental frequency and unwanted harmonics, followed by a matching transformer.

- A half-wave filter is ideal for the output; it consists of a cascade of alternating high- and low-impedance transmission-line sections, each λ/4 long at fo; these sections are λ/2 long at 2*fo and 3λ/4 long at 3*fo. So, the frequencies of maximum rejection occur at fo and 3*fo, but the filter has no rejection at the output frequency 2*fo.
- The imperfect output termination could make the multiplier unstable and cause fundamental frequency leakage.

The **Narrow-band Frequency Doubler** presented below contains the matching transmission line elements TL1 and TL2, and the bias filter elements TL3 and TL4.
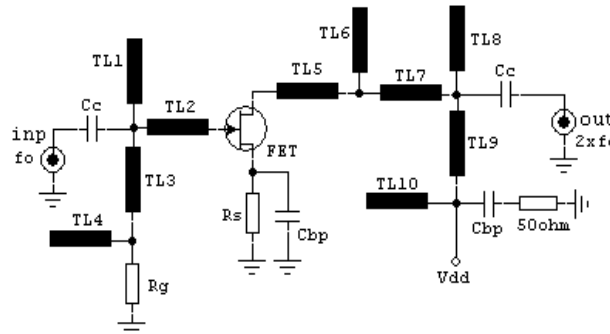
Single Ended Frequency Doubler – Narrowband

- The drain circuit use the transmission line phase-shifter TL5 to adjust the phase of the fundamental frequency impedance, and a harmonic band pass filter.
- The output BPF it is composed of λ/4 transmission lines TL6, TL7 and TL8, which block the fundamental frequency and the 3rd harmonic, and present 50 ohms termination at the 2nd harmonic.
- The electrical angles (phase) of the gate and drain transmission lines, TL5 and TL6, affect the multiplication gain up to 3dB.
- The drain bias filter is composed of elements TL9 and TL10 and their function is to isolate the bias from the generated 2nd harmonic.
- The RC circuit in parallel with the power supply is for overall stabilization.

The **Wide-band Frequency Doubler** presented below use a transmission line (TL5) in series with the output BPF to adjust the phase of the impedance at the fundamental frequency.
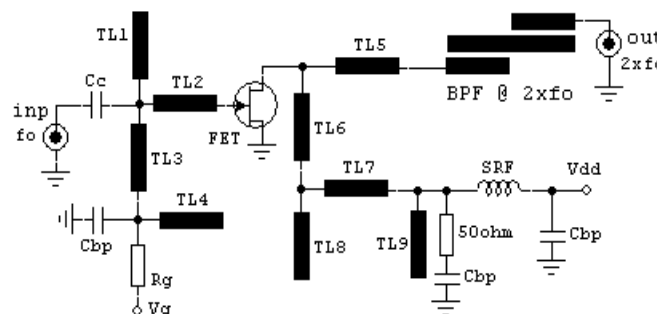

Single Ended Frequency Doubler - Wideband

The BPF rejects the fundamental and the 3rd harmonic frequencies. There is also a band-stop filter (TL7, TL8, TL9) which blocks the 2nd harmonic, and presents low-loss at fundamental and 3rd harmonic.

Frequency FET Triplers

An important difficulty in frequency triplers is the need to short circuit the drain at the unwanted harmonics.
- For example a frequency doubler is easy to do using a λ/4 stub, which effectively shorts the first and third harmonic, while the fourth and higher harmonics are weak enough to neglect.
  But is not very simple for terminating the drain in a frequency tripler.
- The output network can be difficult to design; the inevitable result is a suboptimum termination, which makes very hard to optimize efficiency and get the risk of instability.

This is an example of a FET frequency tripler:
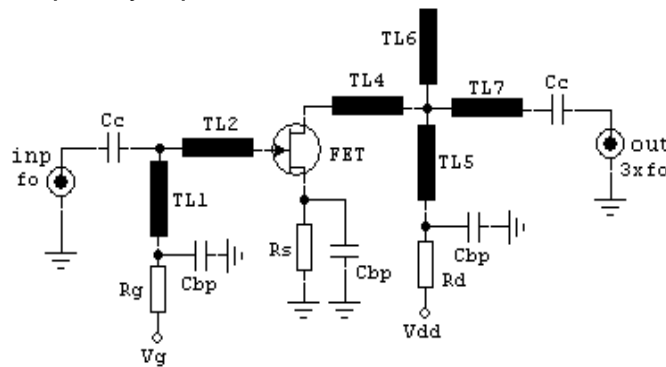
FET Frequency Tripler

- The input stub, grounded at high frequencies by a capacitor, provides a match for the fundamental input frequency, while in the same time it facilitates bias injection at the gate of the FET device by providing some decoupling.
- The bias scheme adopted for the frequency tripler was a self-bias arrangement with resistor between source and ground. Such a self-bias configuration tends to bias a FET device towards pinch-off, with the resistor value determining how close the device is to pinch-off. The larger the value of the closer the bias point is to pinch-off. If the gate bias is connected to an external supply, an option effectively to over-write the self-bias setup is made available.
- At the output, a double stub arrangement has been placed. These stubs get multiple functions. First, they form an output match for the desired 3rd harmonic signal. Secondly, they implement some filtering of undesirable fundamental and 2nd harmonic leakage to the output. Using here the real life stubs, it can be difficult to filter the fundamental without rejecting the desired 3rd harmonic at the same time. This happened when considers the simplest stub arrangement to reject the fundamental, which is an open circuit λ/4 stub. However, such a stub is long 3λ/4 at the 3rd harmonic and tends to reject this frequency as well. As a consequence, the design of the output stub pair involved a compromise in terms of fundamental and 2nd harmonic rejection, without excessively loading the 3rd harmonic response.
- The output stubs is essentially a short circuit stub, the high frequency short being provided by a capacitor to ground. This stub also facilitates drain bias injection.
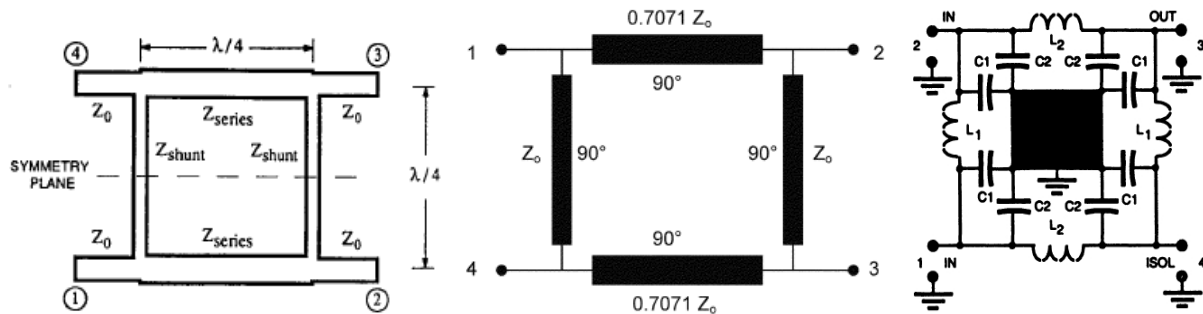
Balanced Frequency Multipliers

Reasons using of Balanced Frequency Multipliers are:
- they have improved input match over wide bandwidth,
- they have good isolation between multiplier stages,
- they are very stable since the device is terminated in 50 ohms over a wideband frequency.
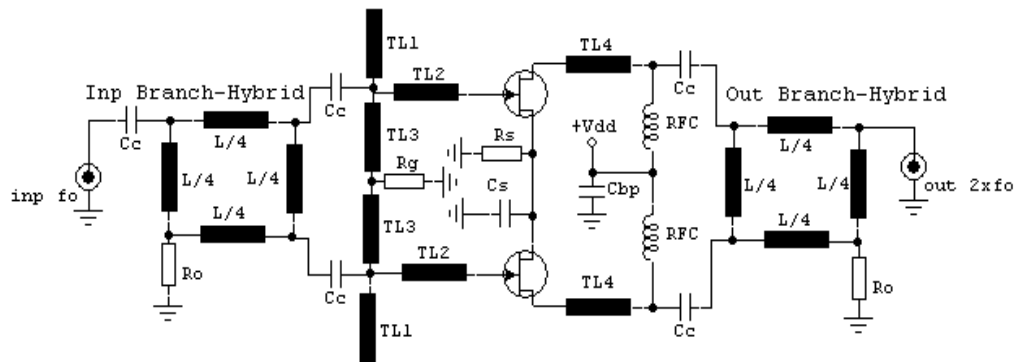
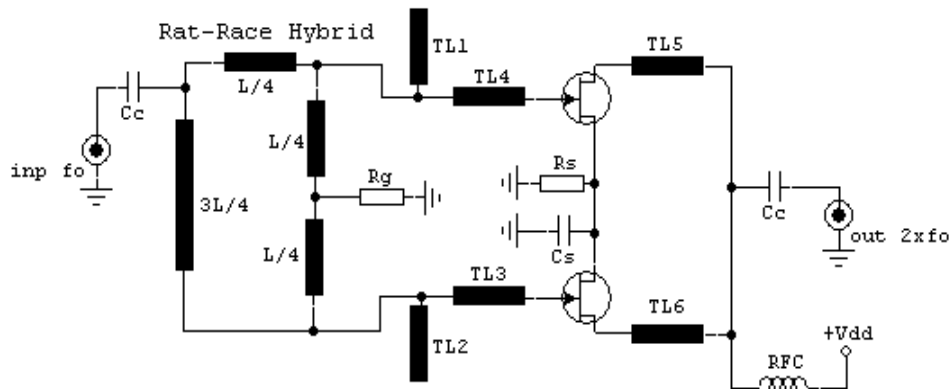Balanced Frequency Doubler using Branch Line Hybrids

Branch Line Hybrid and the Distributed and Lumped equivalents

- The input hybrid coupler introduces a 90° phase shift and the output hybrid another 90°.
- Therefore, the odd harmonics are 180° out of phase, are cancelled at the output port, and dissipated at the coupler termination.
- The even harmonics at the output port are in phase and added in power.
- A balanced multiplier has 3dB greater output power than an equivalent single-device circuit.
- The main bandwidth limitation is given by the FETs input and output matching networks not matched for wideband response.
- The circuit is self-biased using TL3 and Rg gate to the ground and Rs as source resistor. The bias is chosen to be near pinch-off point.

Balanced to Unbalanced Frequency Doubler

Another option is to use only at the input a 180° Rat-Race hybrid to drive each device in anti-phase.
- In this way the fundamental drain currents are also in anti-phase and good rejection is obtained by paralleling both drains, and the drain connection point becomes a virtual ground for fundamental and for all odd harmonics.
- The even harmonics of the drain currents in the two FETs have no phase difference, however, so the drain-current components at those frequencies combine in phase at the output.

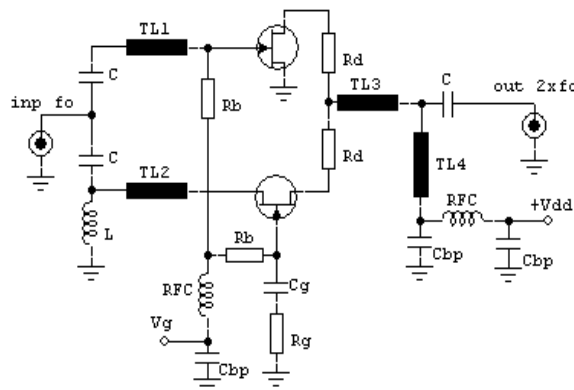Balanced to Unbalanced Frequency Doubler using Rat-Race Hybrid
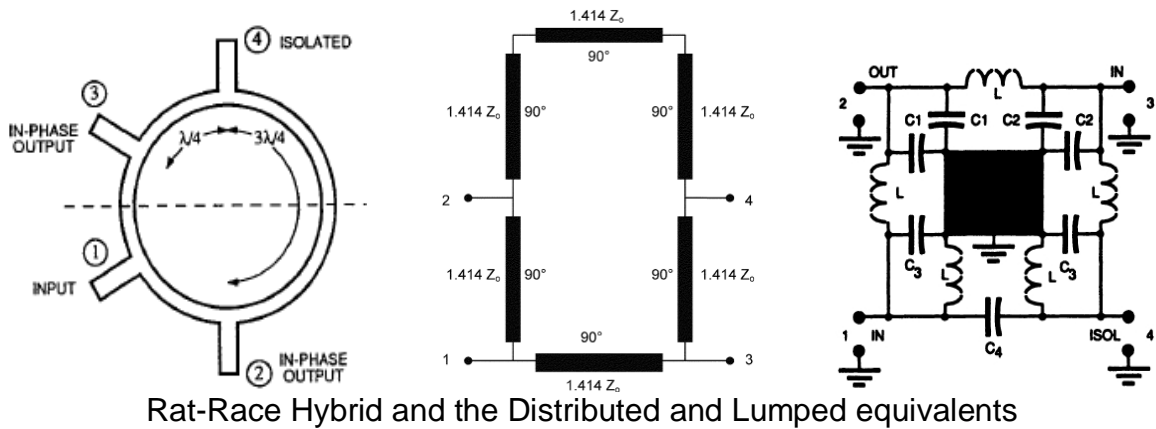
Rat-Race Hybrid and the Distributed and Lumped equivalents

- To get a constant gain at the output, the gates matching networks are designed for maximum gain at fundamental high-end and around 3dB less gain at the low-end of the useful band.
- The disadvantage of this topology is sensitivity to device DC imbalances and input matching networks, compared to the balanced multiplier using hybrids at both, input and output.
- Any imbalance is reflected back to the generator requiring an attenuator at the input to minimize the resulting standing wave.

Balanced Frequency Doubler using Active Balun

The frequency doubler using an active balun presented below is suitable for small size circuits, replacing the passive balun topologies.


Balanced Frequency Doubler using Active Balun

In this frequency doubler, a simple combination of Common-Gate FET and Common-Source FET provides the required 180° phase difference for the cancellation of the fundamental.

- This active balun has the advantage getting small size at low frequencies.
- The stability has to be controlled, in contrast to a passive balun, and the circuit should be unconditionally stable for all input impedance attached.
- To get unconditional stability and to avoid negative resistances at gate and drain of the Common-Gate FET, a series resistance Rg, is added to gate. This reduces the gain, but it improves stability by decreasing the loop gain at the same time. In addition, two series resistors Rd are added in both drain connectors to decrease the loop gain.
- The frequency doubler has a short-circuited stub TL4 and a series transmission line TL3 for an output impedance adjustment at the connection of the two drains. These elements provide a short for the fundamental and additional match for the 2nd harmonic.
- The bias point was chosen at Vg=0 to obtain high fundamental suppression and 2nd harmonic.

Balanced Frequency Tripler

Balanced Frequency Tripler
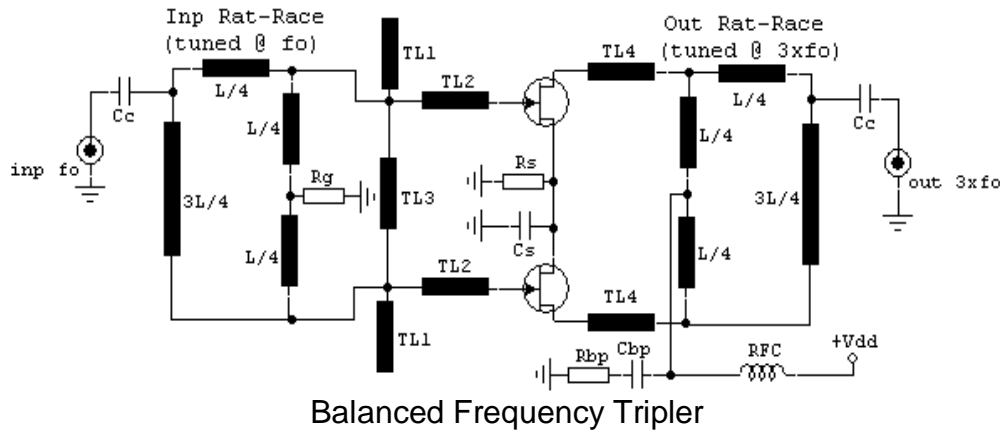
- The input match is made with open-circuited stubs TL1, and high-impedance lines TL2.
- The λ/4 TL3 connecting both inputs introduces a short at the 2nd harmonic, improving the performance.
- The output match contains only a λ/4 high impedance transmission lines TL4, to parallel tune the drain output impedance at the fundamental frequency.
- The device is self-biased and the source resistor Rs is decoupled with Cs.

Higher Order FET Frequency Multipliers

- The direct generation of harmonics of higher order can be obtained by biasing the device at different conduction angles.
- For even order the device is biased in Class-AB similar for frequency doubler, in order to maintain a rectified sinusoidal drain current which is reach in even harmonics.
- For odd order harmonics the optimum bias condition is the one that generates an output waveform with distorted positive and negative peaks. The first option would be to bias the device in Calss-A, about the center of the drain current, and apply a high power at the gate.
- The magnitude of higher harmonic components like 5th, 6th, 7th, etc, becomes too small, requiring a high load resistance to compensate the reduction in output power.

BJT Frequency Multipliers

The theory of bipolar multipliers is essentially the same as that of FET multipliers. A few notes on the differences, however, are in order.
- Unlike FETs, whose channel currents are limited to a little over *Idss*, bipolar devices do not have such a strict limit.
- Silicon BJTs experience high-level injection effects, which tend to limit the peak current and reduce transconductance at high collector current.
- Bipolar devices have a large, strongly nonlinear base-to-emitter capacitance. Because of that capacitance, BJT multipliers are susceptible to modes of oscillation that are not unlike those of junction varactor multipliers for example. As with varactors, the best (and simplest) way to avoid such instability is to short-circuit the base and drain at all unwanted harmonics. Have to verify also that active DC bias supplies do not exhibit negative resistance or couple the collector to the base at low frequencies.
- Because multiplying devices are turned off under quiescent conditions, BJT multipliers should not be current-biased; they must be biased from a voltage source, ideally with a series resistance.

BJT Frequency Tripler
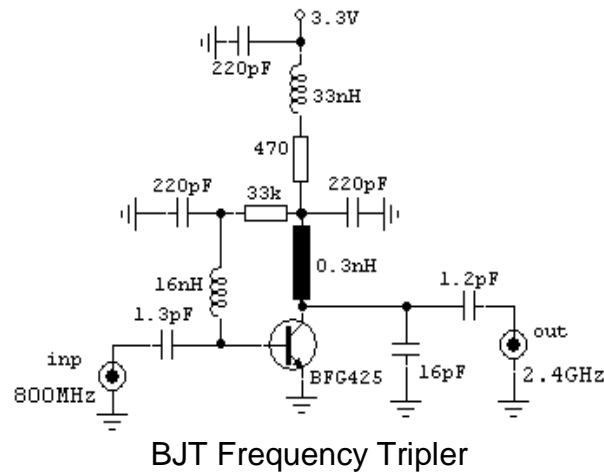
Balanced Push-Push Harmonic Oscillator

Another option generating high frequency signal, using most of the characteristics of the frequency multipliers, is the Harmonic Oscillator.

Below is presented an example of a balanced harmonic oscillator.
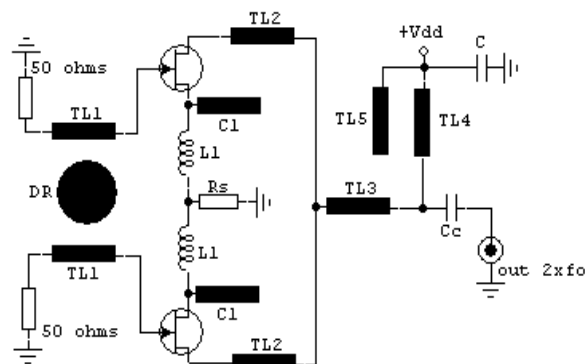
Balanced Push-Push Harmonic Oscillator

- The push-push harmonic oscillator employing two transistors, each oscillating at one half the desired output frequency.
- The transistors oscillate out-of-phase with respect to each other, causing the fundamental frequency to cancel and the second harmonic to add in phase.
- Push-push designs have several advantages over other topologies. Designing at one half the frequency increases resonator Q, decreases the parasitics which appeard, and extends the useful frequency range of transistors.
- The dielectric resonator is placed between the two gates transmission lines (TL1)
- Biasing the circuit in Class-AB, guaranties the start-up and stable oscillation, and also the generation of even harmonics at the output.

Refrences:

1. *Design of FET Frequency Multipliers and Harmonic Oscillators – E. Camargo*
2. *Nonlinear Microwave and RF Circuits – S. Maas*
3. *The RF and Microwave Circuit Design Cookbook – S. Maas*
4. *Microwave and Millimeter-Wave Diode Frequency Multipliers – M. Faber, J. Chramiec, M. Adamski*
5. *Microwave Communications Engineering - Volume 1 – I.A. Glover, S.R. Pennock, P.R. Shepherd*
6. *Millimeter-Wave Integrated Circuits – E. Carey, S. Lidholm*
7. *Varactor Frequency Tripler – R. Zingg*
8. *New Topology Multiplier Generates Odd Harmonics – C. Wenzel*
9. *Choosing a Frequency Multiplier's Waveform – C. Wenzel*
10. *A Highly Integrated Ka- band MMIC Quadrupler – K. Kamozaki, T. Bos, E. Camargo*
11. *Low Cost Frequency Multipliers Using Surface Mount PIN Diode – Application Note – Agilent*
12. *RF Design Magazine, 1990 – 2005*
13. *Microwave Journal Magazine, 1996 – 2010*
14. *High Frequency Electronics Magazine, 1996 – 2010*
15. *Microwaves & RF Magazine, 2000 – 2010*