Linear Front End Module for 4G/5G LTE Advanced Applications

Florinel Balteanu

Skyworks Solutions, Inc., Irvine, CA92617, USA

Florinel.balteanu@skyworksinc.com

***Abstract* — With explosive band proliferation as well the use of carrier aggregation (CA), multiple input multiple output (MIMO) techniques and 5G, research in the area of improving the cost, performance and the size of RF transmit solutions is very active with many developments over the past few years. The proliferation of worldwide smartphones has been in part possible due to increase computational power of CMOS technology in lower feature nodes as 7nm/14nm. This has also made it possible to enhance RF CMOS through digital signal processing (DSP) and digital calibration. Despite this progress there is a shift in terms of what parts of the RF system are portioned in advanced CMOS nodes and what blocks are left and integrated together with other analogue and RF blocks in a front-end module (FEM). This paper proposes a solution for this partitioning for lower cost and size and with high linearity performance and low noise which is mandatory for new 4G/5G multimode multiband (MMBA) FEM module. A 2.3GHz - 2.7GHz broadband CMOS FDD/TDD LTE Band 7, 38, 40 and 41 power amplifier (PA) fully integrated with a fast envelope tracker (ET) on a single 0.18µm CMOS die is presented, as well a method to integrate with a 4G/5G FEM. The CMOS PA and the tracker achieve a 37% overall efficiency for 26.5dBm and -39dBc ACLR1. This paper also presents how this module integrates into a full 4G/5G FEM for mobile applications.**

***Keywords* — CMOS, GaAs, field effect transistor (FET), silicon on insulator (SOI), through wafer via (TSV), long term evolution (LTE), LTE advanced, power amplifier, envelope tracking (ET), multimode multiband front end module, RF front end (RFFE), frequency duplex division (FDD), time division duplex (TDD), digital signal processing (DSP), MIMO, transmit (Tx), carrier aggregation (CA), high power user equipment (HPUE), multi-chip-module (MCM), 4G, 5G.**

I. Introduction

The growing demand for high data rate and longer battery life in communication cellular systems is pushing the rapid adoption for 5G long term evolution (LTE) with rapid deployment and replacement of the already old 3G/4G systems. Also the demand for high data rate as well geographical coverage has increased the number of bands required to be used in a mobile smartphone device; these currently there are more than 40 LTE bands from 700MHz to 5GHz. In parallel there are other radio and bands used in the same time such as WiFi (2.4GHz/5GHz), GPS (1.57GHz), Bluetooth (2.4GHz) and NFC (13.56MHz). These radios have to share common antennas and need to operate without jamming the other device radios. From this perspective a high linearity transmitter and FEM are required together with multiple filters. Fig. 1 presents a typical FEM which covers the LTE FDD/TDD high Bands (HB_LTE) 7, 38, 40 and 41. Also the module has to coexist, operate and reuse the same antennas without jamming the 2.4GHz WiFi bands as well the new 5G LTE bands, such as 3.2GHz-4.9GHz.

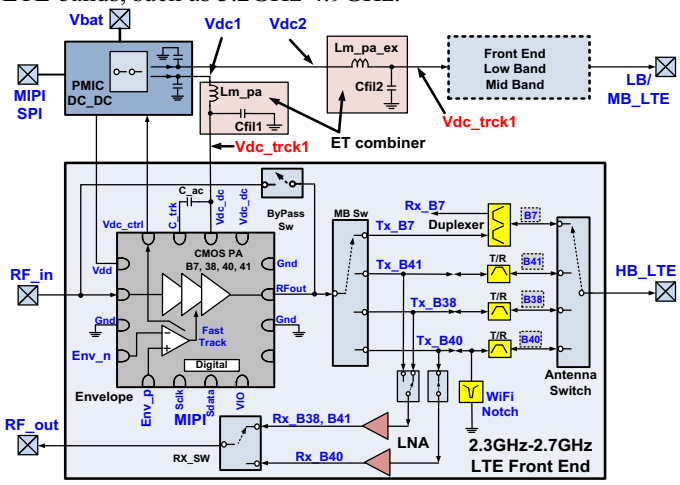

Fig.1. High band 2.3GHz-2.7GHz multimode multi band FEM.

For this reason the FEM has to be very linear and therefore the adjacent channel rejection (ACLR) and noise requirements are very challenging. In Fig. 2 the frequency allocation for 2.3GHz-2.7GHz cellular space and the sharing for 2.4GHz WiFi space are presented.

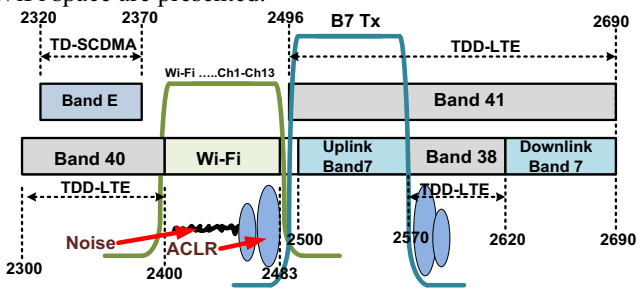

Fig.2. High band 2.3GHz-2.7GHz LTE frequency bands

The Band 7 FDD transmitter as well Band 40 and Band 41 both operating as TDD require higher ACLR to relax the filter requirements for coexistence with 2.5GHz WiFi channels.

Fig. 3 presents the typical 4G/5G integration into a smartphone for 2.3GHz-2.7GHz FEM. The adoption of 5G uplink/downlink where 2 to 6 more transmit/receive channels operate at the same time increases the linearity and noise requirements of the FEM integration.

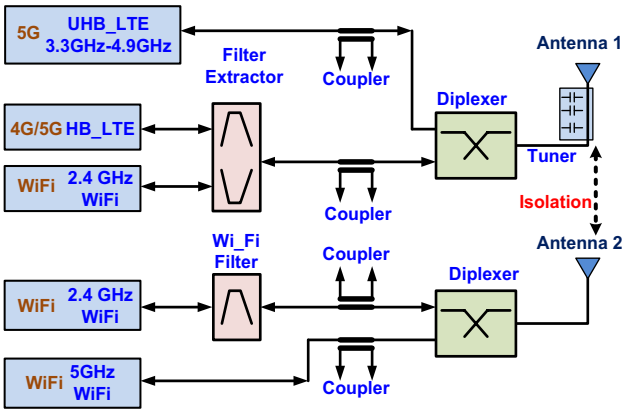

Fig.3. 4G/5G RFFE module integration.

The cellular LTE bands use complex digitally modulated signals, such as 16/64QAM and place stringent linearity demands on the RF power amplifiers (PAs) to achieve high efficiency and high linearity for a wide power range, as presented in Fig.3. To increase the data stream bandwidth 5G will use modulations such as DFT-S-FDM and CP-OFDM modulation up to 256QAM with 10.5dB peak-to-average ratio (PAPR) [1]. For higher modulation rate (64/256QAM) there is maximum power reduction (MPR) of 3-5dB. Typically to operate a power amplifier under high PAPR the amplifier is operated under back off mode which reduces the efficiency (Fig.4); For example, a typical WiFi PA operated at 256QAM and 8.5dB PAPR ends up with power added efficiency (PAE) around 12%-15%.

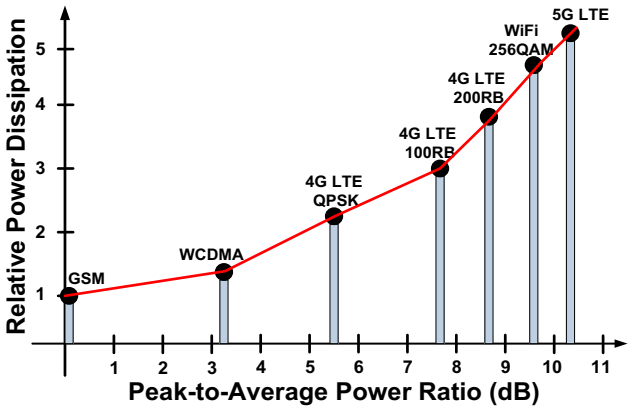

Fig. 4. Peak-to-average power ratio.

For a typical linear PA operating in class B mode when the active device conducts 180° the maximum output power is given by

$$Pout\_\max = \frac{(Vdd - Vkn)^2}{2Rlopt} \qquad (1)$$

where *Rlopt* is the optimum impedance which has to be matched at the output load through the marching network and *Vkn* is the knee voltage. If the PA is operated in ET mode, *Vdd=Vdc_trck* is changing based on the envelope (instantaneous power level). The *Vdc_trck_peak* is the peak voltage and is determined by the maximum power which has to be delivered under ET for different PAPR waveforms

$$PAPR = 20\log(\frac{Vdc\_trck\_peak}{Vdc\_trck\_rms}) \qquad (2)$$

For 5G the duplexer loss in FDD-LTE systems makes TDD-LTE systems a better candidate, assuming higher PAPR signal coding up to 10.5dB. TDD-LTE systems with asymmetrical uplink/downlink ratio (such as 1/3) stress more the transmit uplink chain. In this scenario for TDD-LTE the bandwidth requirements to have the same uplink data stream throughput is at least five times higher assuming the required gaps in uplink TDD. Therefore at least 40MHz TDD-LTE is required to reach a similar peak bandwidth as for 10MHz FDD-LTE. Noise power is proportional to bandwidth and therefore the TDD power required to have the same signal to noise ratio (SNR) like in FDD is given by Eq. 3

$$Pout(TDD) = Pout(FDD) + 10\log(Bw\_ratio) \qquad (3)$$

Assuming Eq. 3, for TDD-LTE operation the PA has to deliver 27dBm to achieve the same SNR as a 20dBm LTE FDD signal, considering the same propagation environment. From this perspective for higher modulation bandwidth (4G/5G LTE) the PA operates most of the time at peak power as compared with old 3G WCDMA systems where the PA operates in back-off mode.

II. Front End Module Structure

The FEM configuration and design are determined by cost, size and RF performance. With the adoption of 5G where two or more transmitters are active at a time the linearity requirements such as ACLR and noise are tightened. Adjacent channel interference ratio (ACIR) is the total leakage between two transmitters on adjacent channels which depends on ACLR and adjacent channel selectivity (ACS) as defined by

$$ACIR = \frac{1}{\frac{1}{ACLR} + \frac{1}{ACS}} \qquad (4)$$

To increase ACIR is desired to have an ACLR better than -38dBc, usually lowered to -45dBc using ET and DPD. Fig. 5 presents the power budget for FEM transmit path, the loss for this path typically being around 3dB. This loss increases for 5G application when a diplexer (0.3dB) and/or a dual pole dual through DPDT SOI switch are added. For LTE 5G there is also a 3dB increase of the uplink power for HPUE which allows a better balanced downlink and uplink coverage in TDD.

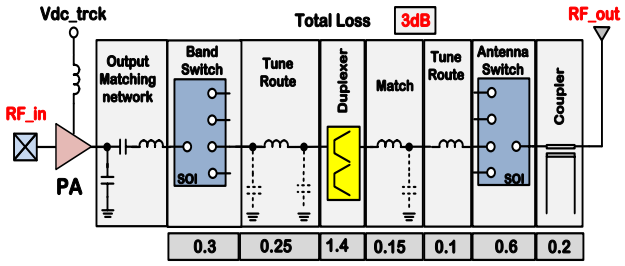

Fig. 5. FEM power loss budget.

III. Power Amplifier Circuitry

To reduce the FEM size, the PA design uses a 0.28um CMOS. Using CMOS for PAs has several challenges due to the lower transistor breakdown voltage and reduced intrinsic linearity for CMOS transistors compared with GaAs. To overcome this, CMOS PAs for LTE use ET [2] to increase linearity and efficiency. ET used with CMOS PAs increase the ACLR and error vector magnitude (EVM) to higher degree than for a GaAs PAs.

For GaAs HBT technologies a semi-insulating substrate is used so devices fabricated will have reduced parasitic capacitances and higher Ft devices. Also GaAs technologies usually feature backside TSVs that connect the front side metallization of the die to the back side ground plane. These features provide a low impedance path to the common ground plane and a good thermal conductor.

In order to deal with these limitations, the CMOS PA designs have used flip-chip techniques and laminate substrate for output matching networks. Still losses and size for CMOS and CMOS-SOI PAs using flip-chip are higher than GaAs PAs. For these reasons, this design uses High Resistivity CMOS substrate (3kohm) and Through Wafer Vias (TSVs) as presented in Fig. 6.

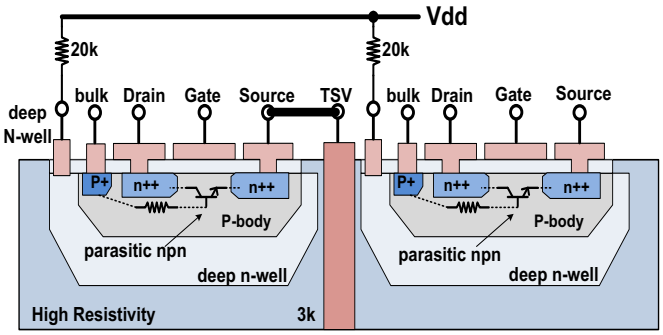

Fig.6 CMOS PA transistor structure.

The most difficult issue with CMOS technology scaling is the need to overcome the overvoltage stress. Using stacked cascode transistors has the benefit of improving the reliability of CMOS PAs. Fig. 7 shows the block diagram of the implemented CMOS PA with the tracker integrated on the same die.

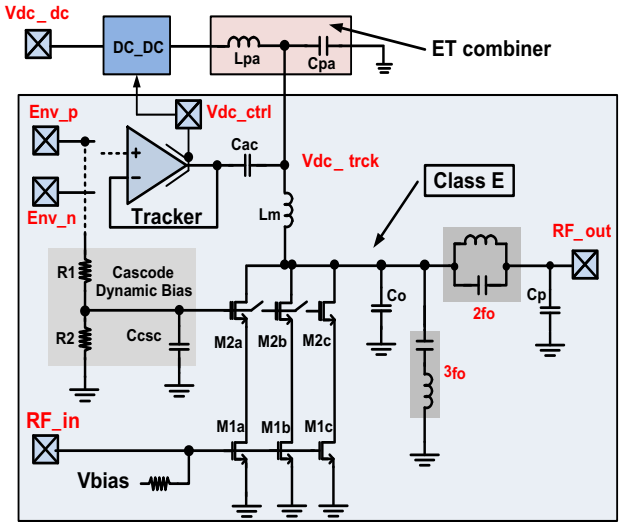

Fig. 7. Broadband class E CMOS PA and tracker

The PA has been designed with two stages both using 1.8V/3.3V cascode structures. The use of low feature size 1.8V transistors for RF drive (M1) does help to increase the RF gain and PA efficiency. The top transistors (M2) are thick gate 3.3V CMOS which handle the high voltage stress. All the power transistors sit in separate deep n-well to increase linearity through extending the breakdown CMOS region [3], as presented in Fig. 7. In order to provide broadband characteristic the PA is using a CMOS class-E structure with additional third harmonic 3fo trap [4], [5]. Then to improve the power added efficiency PAE and linearity a fast envelope tracker has been integrated on the same die with the PA. The fast tracker works together with a buck DC_DC converter, providing approximatively 20% of the power required by the PA. For an output power of 26.5dBm the buck DC voltage Vdc-dc is set at 2.7V and provides the 80% of the PA power with more than 94% efficiency. This DC low voltage provides protection for CMOS devices but it does require the PA to operate at low load line. The envelope signal is used to dynamical bias the top cascode transistor and keeps the main RF transistor in the approximate constant *gm* region.

IV. Switch Circuitry

The RF switches have been integrated as separate dies to increase isolation and use SOI technology for low insertion loss (IL). One arm switch structure is presented in Fig. 8.

Assuming equal voltage division for each SOI FET the peak RF voltage across drain-source for each transistor V_{DS}_peak is

$$\left|V_{DS\_peak}\right| = 2(V_{Th} - V_{NEG}) \qquad (5)$$

where *Vneg* is the negative voltage generated through a charge pump.

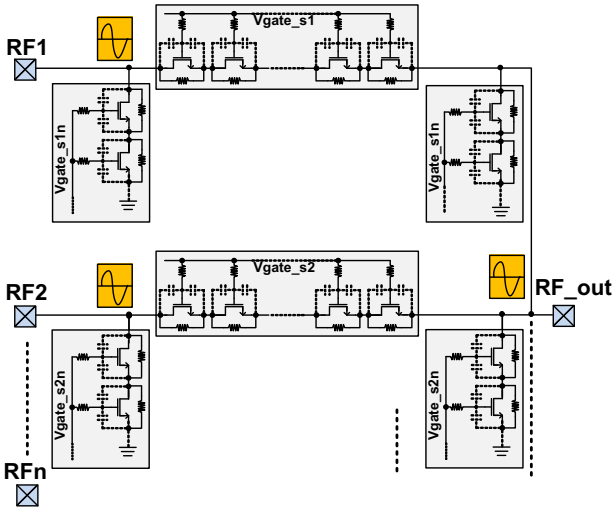

Fig. 8. SOI switch structure.

The number of the series FETs (n) is determined by the maximum peak RF power *Pmax* applied to the switch and the breakdown requirements for CMOS/SOI transistors as expressed by

$$P_{\max} = \frac{V_{Tx\max}^2}{2 * Z_0} = \frac{2(nV_{DS\_peak})^2}{Z_0} \qquad (6)$$

V. Calibration and Measurements

The FEM working with ET requires delay calibration for the envelope and RF signal. The module includes high Q filters and for this reason a new calibration method where a slow envelope signal is aligned through convolution method with a RF signals pushing the PA in compression has been used. The CMOS PA and ET die (1.6mm x 1.7mm) has been packaged together with SOI switches, filters and in an multi-chip-module (MCM) package. The chip photographs for CMOS PA and 4T1P SOI switch are presented in Fig. 9.

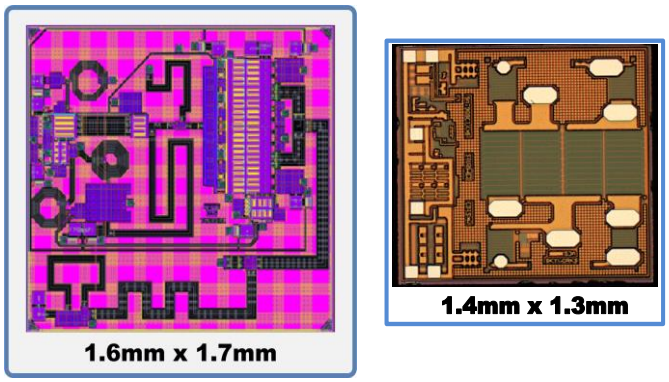

Fig. 9. CMOS PA and SOI switch photographs.

Tested with a 20MHz, 100RB LTE signal the overall system efficiency observed was 36.5% at 26.5dBm for ACLR1 of -39dBc and ACLR2 of -50dBc, without DPD, as presented in Table 1. In Table 2. measurements are presented for a 4P1T SOI antenna switch.

Table 1. Results for 2.5GHz, LTE 20MHz, Band7

Pout (dBm)	Vdc_dc (V)	ACLR (dBc)	Eff (%)	RxBN@30MHz (dBm/Hz)
26.5	2.7	-39	36.5	-123.4
28	3.1	-34	39	-123.1
29	3.4	-31	41	-120.5

Table 2. 4P1T SOI Switch Measurements Results.

Insertion loss at 2.5GHz	**0.6dB**
Isolation	**21dB**
IIP2	**95dBm**
IIP3	**84dBm**
Switching Speed	**2µs**
Supply Current	**28µA**

VI. Conclusions

A fully integrated 0.18µm 2.3GHz-2.7GHz broadband CMOS PA and ET was packaged together with SOI switches and filters into a FEM and its performance characterized. The SOI 4P1T switch measurement has been presented as well The integration of the fast tracker into FEM opens the possibility for two or more uplink Tx to operate at the same time which is the case for future 4G/5G LTE advanced versus present mobile applications.

References

[1] D. Pehlke, D. Brunel, K. Walsh, S. Kovacic, "Sub-6GHz 5G for UE, Optimizing Cell Edge User Experience," *IWPC 4G/5G Multi-band, Multi-Mode User Equipment*, Austin, October 2017.

[2] Y. Li, J. Lopez, C. Schecht, R. Wu and D. Lie, "Design of high efficiency monolithic power amplifier with envelope-tracking and transistor resizing for broadband wireless applications," *IEEE Journal of Solid-State Circuits,* vol. 47, no.9, pp.2007–2018, September 2012.

[3] J. Kang, D. Yu, Y. Yang, and B. Kim, "Highly Linear 0.18-µm CMOS Power Amplifier With Deep n-Well Structure," *IEEE Journal of Solid-State Circuits,* vol. 41, No.5, pp. 1073–1080, May 2006.

[4] A. Grebennikov, "High-efficiency class E/F lumped and transmission line power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, pp. 1579-1588, June 2011.

[5] A. Mazzanti, L. Larcher, R. Brama, F. Svelto, "Analysis of Reliability and Power Efficiency in Cascode Class-E PAs," IEEE *Journal of Solid-State Circuits,* vol. 41, No.5, pp. 1222–12290, May 2006.